Chapter 4

SYSTEM MODULE

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CHAPTER 4 – SYSTEM MODULE

Contents

Introduction

GT8 is the baseband/RF module NHE–5 cellular tranceiver. The GT8 module carries out all the system and RF functions of the tranceiver. System module GT8 is designed for a handportable phone, that operate in GSM system.

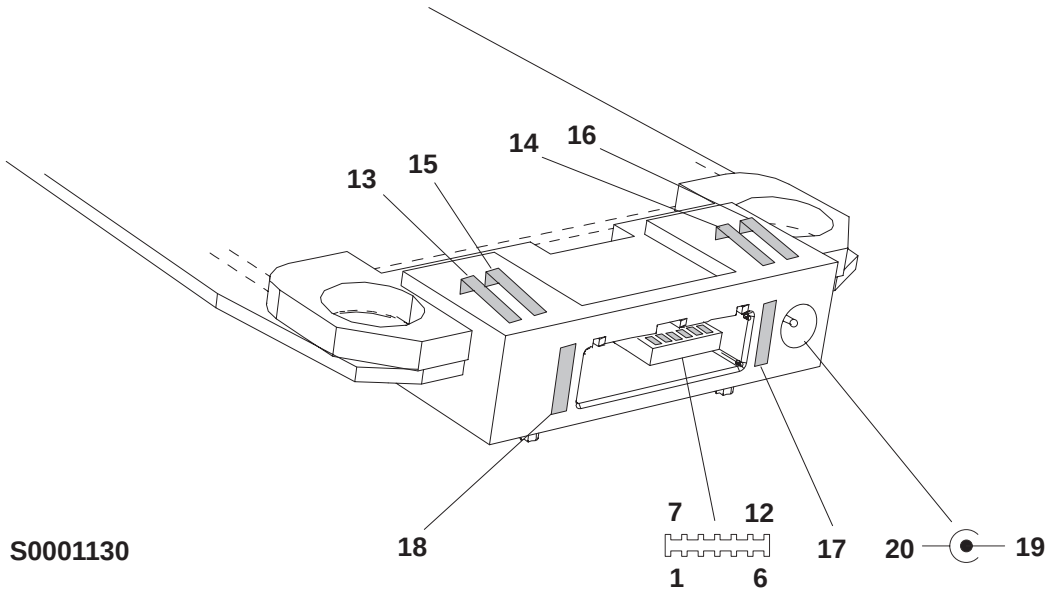
Technical Section

All functional blocks of the system module are mounted on a single multi layer printed circuit board. The chassis of the radio unit has separating walls for baseband and RF. All components of the baseband section are surface mountable. They are soldered using reflow. The connections to accessories are taken through the bottom connector of the radio unit. The connections to the User Interface module (UIF) are fed through a connector. There is no physical connector between the RF and baseband sections.

External and Internal Connections

The system module has two connector, external bottom connector and internal display module connector.

System Connector X103



Accessory Connector

Pin:	Name:	Description:
1	GND	Digital ground
2	V_OUT	Accessory output supply • min/typ/max: 3.25...10 V (output current 50 mA)
3	XMIC	External microphone input and accessory identification • nom/max: 8...50 mV (the maximum value corresponds to 0 dBm network level with input amplifier gain set to 20 dB, typical value is maximum value –16 dB)
	ID	Accessory identification • 1.7...2.05 V headset adapter connected • 1.15...1.4 V compact hadsfree unit connected
4	NC	No connection
5	NC	No connection
6	MBUS	Serial control bus • logic low level: 0...0.5 V • logic high level: 2.4...3.2 V
7	NC	No connection
8	SGND	Signal ground
9	XEAR	External audio output and mute control • min/nom/max: 0...32...500 mV (typical level correnspondsto –16 dBm0 network level with volume control in nominal position 8 dB below maximum. Maximum 0 dBm0 max. volume codec gain –6 dB) • mute on (HF speaker mute): 0...0.5 V d.c. • mute off (HF speaker active): 1.0...1.7 V d.c.
10	HOOK	Hook control, accessory connection detect • hook off (handset in use) : 0...0.5 V • hook on, (handset not in use): 2.4...3.2 V
11	NC	No connection
12	V_IN	Charging supply voltage • max: 16 V

Battery Connector

Pin:	Name:	Description:
13	BGND	Battery ground
14	BSI	Battery size indicator (used also for SIM card detection) • R2=47k pullup resistor in module
15	BTEMP	Battery temperature (used also for vibration alert) • 47 kΩ NTC in battery to gnd, 47 kΩ pullup in module
16	VB	Battery voltage • min/typ/max: 5.3...6...8.6 V

Charging connectors

Pin:	Name:	Description:
17, 19	V_IN	Charging voltage input • ACH–6 min/nom/max: 9.8...10.3...10.8 V • ACH–8 min/nom/max: 12...14...16 V
18, 20	GND	Charger ground

UI Connector X101

Pin:	Name:	Description:
1	EARP	Earphone positive signal • min/typ/max: 0...14...220 mV (typical level correnspondes to –16 dBm0 network level with volume control giving nominal RLR (=+2 dB) 8 dB below maximum. Maximum 0 dBm0 with max. volume (codec gain –11 dB)
2	EARN	Earphone negative signal • min/typ/max: 0...14...220 mV (see above)
3	VBKEY	Battery supply • min/max: 5.3...8.5 V
4	BUZZER	Alert buzzer (audio codec PWM controlled)
5–7	ROW(0–2)	Input
8–10	GND	Shield ground
11–13	ROW(3–5)	Input

Pin:	Name:	Description:
14	LIGHTC	Keyboard light
15–18	COL(0–3)	Output
19	PWRKEY	Power on/off
20	GND	Digital ground

Flash Connector X103

Pin:	Name:	Description:
1	WDDIS	Watchdog disable, signal pulled down to disable watchdog, test point J300
2	FCLK	Flash serial clock, test point J303
3	VPP	Flash programming voltage • min/typ/max: 11.4...12...12.6 V (values when VPP active), test point J304
4	FTX	Flash acknowledge transmit, test point J302
5	FRX	Flash data receive, test point J301

SIM Connector X102

Pin:	Name:	Description:
1	GND	Ground for SIM
2	VSIM	SIM voltage supply • min/typ/max: 4.8...4.9...5.0 V
3	SDATA	Serial data for SIM
4	SRES	Reset for SIM
5	CLK	Clock for SIM data (clock frequency minimum 1 MHz if clock stopping not allowed)

Baseband Block

Introduction

The GT8 module is used in NHE–5 products. The baseband is built around one DSP, System ASIC and the MCU. The DSP performs all speech and GSM/PCN related signal processing tasks. The baseband power supply is 3V except for the A/D and D/A converters that are the interface to the RF section. The A/D converters used for battery monitoring are integrated into the same device as the signal processing converters.

The audio codec is a separate device which is connected to both the DSP and the MCU. The audio codec support the internal and external microphone/ear-piece functions. External audio is connected in a dual ended fashion to improve audio quality together with accessories.

The baseband implementation support a 32 kHz sleep clock function for power saving. The 32 kHz clock is used for timing purposes during inactive periods between paging blocks. This arrangement allows the reference clock, derived from RF to be switched off.

The baseband clock reference is derived from the RF section and the reference frequency is 13 MHz. a low level sinusoidal wave form is fed to the ASIC which acts as the clock distribution circuit. The DSP is running at 39 MHz using an internal PLL. The clock frequency supplied to the DSP is 13 MHz. The MCU bus frequency is the same as the input frequency. The system ASIC provides both 13 MHz and 6.5 MHz as alternative frequencies. The MCU clock frequency is programmable by the MCU. The baseband uses 6.5 MHz as the MCU operating frequency. The RF A/D, D/A converters are operated using the 13 MHz clock supplied from the system ASIC

The power supply and charging section supplies several types of battery technologies. such as , NiCd, NiMH and Lithium. The battery charging unit is designed to accept constant current type chargers, that are approved by NMP.

The power supply IC contains three different regulators. The output voltage from each regulator is 3.15V nominal. One of the regulator uses an external transistor as the boost transistor.

Modes of Operation

The baseband in operates in the following Modes

– Active, as during a call or when baseband circuitry is operating

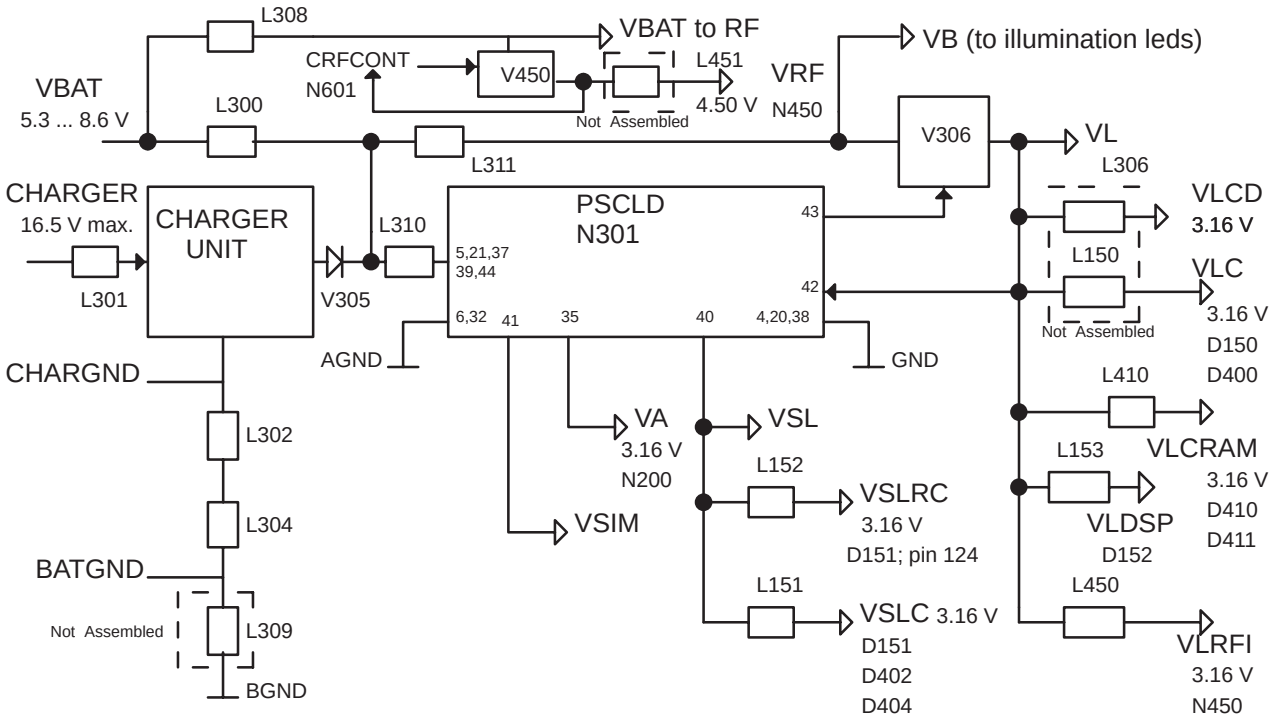
– Sleep, in this mode the clock to the baseband is stopped and timing is kept by the 32 KHz oscillator. All Baseband circuits are powered

– Acting dead, in this mode the battery is charged but only necessary functions for charging are running

– Power off, in this mode all baseband circuits are powered off. The regulator IC N301 is powered

Circuit Description

Power Supply



The power supply for the baseband is the main battery. The main battery consists of 5 NiCd or NiMH cells with a nominal voltage of 6.0V. A charger input is used to charge the battery. Two different chargers can be used for charging the battery. A switch mode type fast charger that can deliver 780 mA and a standard charger that can deliver 265 mA. The idle voltage for the fast and standard charger see NO TAG. Both chargers are of constant current type.

The baseband has one power supply circuit, N301 delivering power to the different parts in the baseband. There are two logic power supply and one analog power supply. The analog power supply VA is used for analog circuits such as audio codec, N200 and microphone bias circuitry. Due to the current consumption and the baseband architecture the digital supply is divided into to parts.

Both digital power supply rails from the N301, PSCLD is used to distribute the power dissipation inside N301, PSCLD. The main logic power supply VL has an external power transistor, V306 to handle the power dissipation that will occur when the battery is fully charged or during charging.

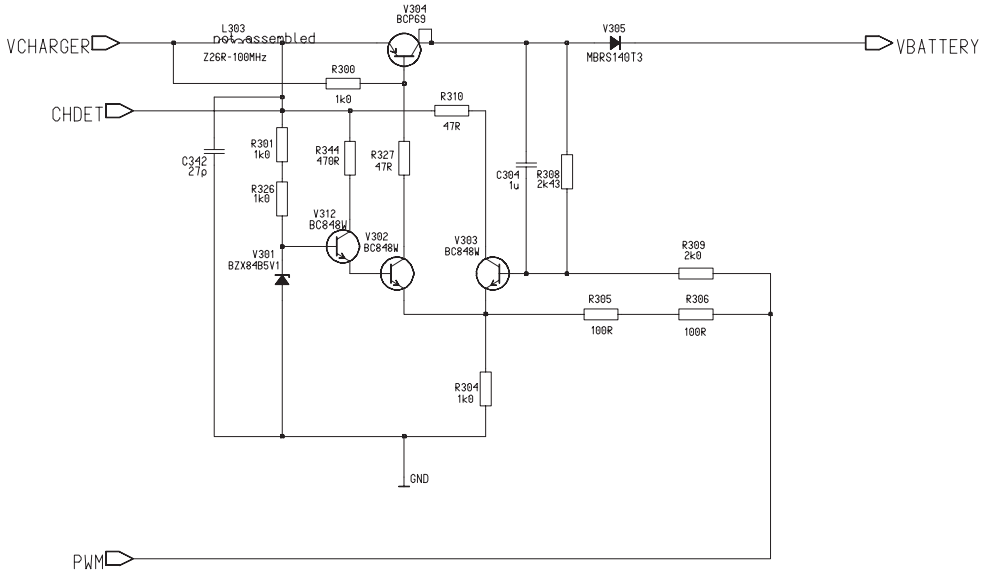
D151, ASIC and the MCU SRAM, D402/D403 are connected to the same logic supply voltage. All other digital circuits are connected to the main digital supply. The analog voltage supply is connected to the audio codec.

Charging Control Switch Functional Description

The charging switch transistor V304 controls the charging current from the charger input to the battery. During charging the transistor is forced in saturation and the voltage drop over the transistor is 0.2–0.4V depending upon the current delivered by the charger. Transistor V304 is controlled by the PWM output from N301, pin 23 via resistors R309, R308 and transistor V303. The output from N301 is of open drain type. When transistor V304 is conducting the output from N301 pin is low. In this case resistors R305 and R306 are connected in parallel with R304. This arrangement increases the base current through V304 to put it into saturation.

Transistors V304, V302, V303 and V312 forms a simple voltage regulator circuitry. The reference voltage for this circuitry is taken from zener diode V301. The feedback for the regulator is taken from the collector of V304. When the PWM output from N301 is active, low, the feedback voltage is determined by resistors R308 and R309. This arrangement makes the charger control switch circuitry to act as a programmable voltage regulator with two output voltages depending upon the state of the PWM output from N301. When the PWM is inactive, in high impedance the feedback voltage is almost the same as on the collector of V304. Due to the connection the voltage on V303 and V302 emitters are the same. The influence of the current thru R305 and R306 can be neglected in this case.

The charging switch circuit diagram is shown in following figure. The figure is for reference only.



This feedback means that the system regulates the output voltage from V304 in such a way that the base of V303 and V302 are at the same voltage. The voltage on V302 is determined by the V301 zener voltage. The darlington connection of V312 and V302 service two purposes 1 the load on the voltage reference V301 is decreased, 2 the output voltage on V304 is decreased by the VBE voltage on V312 which is a wanted feature. The voltage reduction allows a relative temperature stable zener diode to be used and the output voltage from V304 is at a suitable level when the PWM output from N301 is not active.

The circuitry is self starting which means that an empty battery is initially charged by the regulator circuitry around the charging switch transistor. The battery is charged to a voltage of maximum 4.8V. This charging switch circuitry allows for both NiCd, NiMH and Lithium type of batteries to be used.

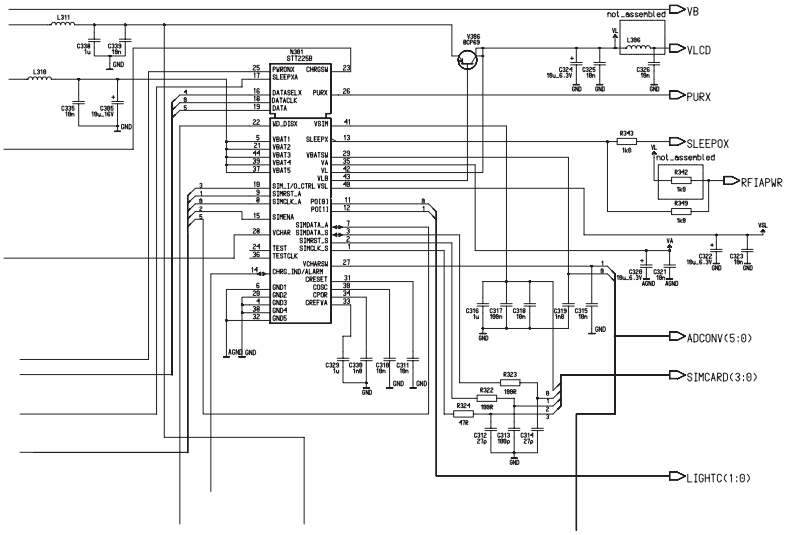
When the PWM output from N301 is active the feedback voltage is changed due to the presence of R308 and R309. When the PWM is active the charging switch regulator voltage is set to 10.5V maximum. This means that even if the voltage on the charger input exceeds 11.5V the battery voltage will not exceed 10.5 V. This protects N301 from over voltage even if the battery was to be detached while charging.

V305 is a schottky diode that prevents the battery voltage from reverse bias V304 when the charger is not connected. The leakage current for V305 is increasing with increasing temperature and the leakage current is passed to ground via R308, V303 and R304. This arrangement prevents V304 from being reversed biased as the leakage current increases at high temperatures.

V300 is a 16V transient suppressor. V300 protects the charger input and in particular V304 for over voltage. The cut off voltage is 16V with a maximum surge voltage up to 25V. V300 also protects the input for wrong polarity since the transient suppressor is bipolar.

Power Supply Regulator PSCLD, N301

The power supply regulators are integrated into the same circuit N301. The power supply IC contains three different regulators. The main digital power supply regulator is implemented using an external power transistor V306. The other two regulators are completely integrated into N301.



PSCLD, N301 External Components

N301 performs the required power on timing. The PSCLD, N301 internal power on and reset timing is defined by the external capacitor C330. This capacitor determines the internal reset delay, which is applied when the PSCLD, N301 is initially powered by applying the battery. The baseband power on delay is determined by C311. With a value of 10 nF the power on delay after a power on request has been active is in the range of 50–150 ms. C310 determines the PSCLD, N301 internal oscillator frequency and the minimum power off time when power is switched off.

The sleep control signal from the ASIC, D151 is connected via PSCLD, N301. During normal operation the baseband sleep function is controlled by the ASIC, D151 but since the ASIC is not power up during the startup phase the sleep signal is controlled by PSCLD, N301 as long as the PURX signal is active. This arrangement ensures that the 13 MHz clock provided from RF to the ASIC, D151 is started and stable before the PURX signal is released and the baseband exits reset. When PURX is inactive, high, sleep control signal is controlled by the ASIC D151.

N301 requires capacitors on the input power supply as well as on the output from each regulator to keep each regulator stable during different load and temperature conditions. C305 and C335 are the input filtering capacitors. Due to EMC precautions a filter using C337, L310, C335, L311, C338 and C339 has been inserted into the supply rail. This filter reduces the high frequency components present at the battery supply from exiting the baseband into the battery pack. The regulator outputs also have filter capacitors for power supply filtering

and regulator stability. A set of different capacitors are used to achieve a high bandwith in the suppression filter.

PSCLD, N301 Control Bus

The PSCLD, N301 is connected to the baseband common serial control bus, SCONB(5:0). This bus is a serial control bus from the ASIC, D151 to several devices on the baseband. This bus is used by the MCU to control the operation of N301 and other devices connected to the bus. N301 has two internal 8 bit registers and the PWM register used for charging control. The registers contain information for controlling reset levels, charging HW limits, watchdog timer length and watchdog acknowledge.

The control bus is a three wire bus with chip select for each device on the bus and serial clock and data. From PSCLD, N301 point of view the bus can be used for writing only. It is not possible to read data from PSCLD, N301 by using this bus.

The MCU can program the HW reset levels when the baseband exits/enters reset. The programmed values remains until PSCLD is powered off, the battery is removed. At initial PSCLD, N301 power on the default reset level is used. The default value is 5.1 V with the default hysteresis of 400 mV. This means that reset is exit at 5.5 V when the PSCLD, N301 is powered for the first time.

The watchdog timer length can be programmed by the MCU using the serial control bus. The default watchdog time is 32 s with a 50 % tolerance. The complete baseband is powered off if the watchdog is not acknowledged within the specified time. The watchdog is running while PSCLD, N301 is powering up the system but PURX is active. This arrangement ensures that if for any reason the battery voltage doesn’t increase above the reset level within the watchdog time the system is powered off by the watchdog. This prevents a faulty battery from being charged continuously even if the voltage never exceeds the reset limit. As the time PURX is active is not exactly known, depends upon startup condition, the watchdog is internally acknowledged in PSCLD when PURX is released. This gives the MCU always the same time to respond to the first watchdog acknowledge.

Baseband power off is initiated by the MCU and power off is performed by writing the smallest value to the watchdog timer register. This will power off the baseband within 0.5 ms after the watchdog write operation.

The PSCLD, N301 also contains switches for connecting the charger voltage and the battery voltage to the baseband A/D converters. Since the battery voltage is present and the charger voltage might be present in power off the A/D converter signals must be connected using switches. The switch state can be changed by the MCU via the serial control bus. When PURX is active both switches are open to prevent battery/charger voltage from being applied to the baseband measurement circuitry which is powered off. Before any measurement can be performed both switches must be closed by MCU.

Charger Detection

A charger is detected if the voltage on N301 pin 28 is higher than 0.5V. The charger voltage is scaled externally to PSCLD, N301 using resistors R302 and R303. With the implemented resistor values the corresponding voltage at the charger input is 2.8V. Due to the multifunction of the charger detection signal from PSCLD, N301 to ASIC, D151 the charger detection line is not forced ,active high until PURX is inactive. In case PURX is inactive the charger detection signal is directly passed to D151. The active high on pin 14 generates and interrupt to MCU which then starts the charger detection task in SW.

SIM Interface and Regulator in N301

The SIM card regulator and interface circuitry is integrated into PSCLD, N301. The benefit from this is that the interface circuits are operating from the same supply voltage as the card, avoiding the voltage drop caused by the external switch used in previous designs. The PSCLD, N301 SIM interface also acts as voltage level shifting between the SIM interface in the ASIC, D151 operating at 3V and the card operating at 5V. Interface control in PSCLD is direct from ASIC, D151 SIM interface using SIMI(5:0) bus. The MCU can select the power supply voltage for the SIM using the serial control bus. The default value is 3V which needs to be changed to 5V before power up the SIM interface in ASIC, D151. Regulator enable and disable is controlled by the ASIC via SIMI(2). For further operation of the SIM interface see section NO TAG.

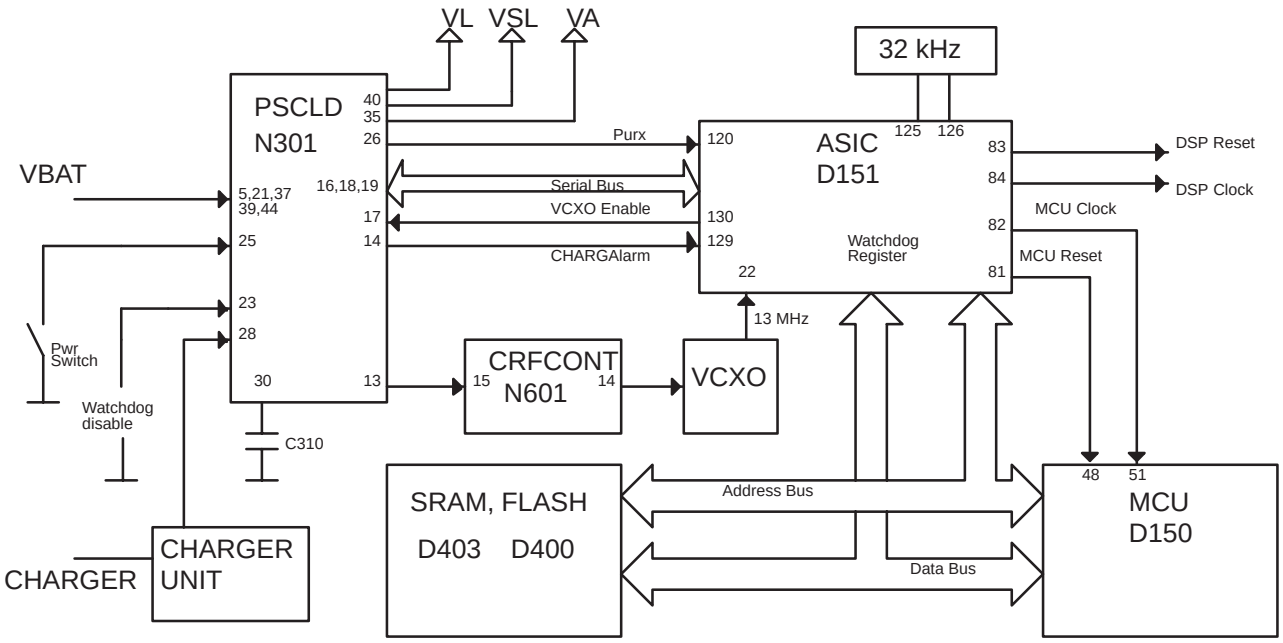
Power Up Sequence

The baseband can be powered up in three different ways.

– When the power switch is pressed input pin 25 to PSCLD, N301 is connected to ground and this switches on the regulators inside PSCLD.

– An other way to power up is to connect the charger. Connecting the charger causes the baseband to power up and start charging the battery.

– The third way to power the system up is to attach the battery.



Power up using Power on Button

This is the most common way to power the system up. This power up is successful if the battery voltage is higher than power on reset level set by the MCU, default value 5.5V in PSCLD, N301. The power up sequence is started when the power on input pin 25 at PSCLD is activated, low. The PSCLD then internally enters the reset state where the regulators are switched on. At this state the PWM output from PSCLD is forced active to support additional power from any charger connected. The sleep control output signal is forced high enabling the regulator to supply the VCO and startup the clock. After the power on reset delay of 50–150 ms PURX is released and the system exits reset. The PWM output is still active until the MCU writes the first value to the PWM register. The watchdog has to be acknowledged within 16 s after that PURX has changed to inactive state

Power Up with Empty Battery using Charger

When the charger is inserted into the DC jack or charger voltage is supplied at the system connector surface contacts/pins PSCLD , N301 powers up the baseband. The charging control switch is operating as a linear regulator, the output voltage is 4.5V–5V. This allows the battery to be charged immediately when the charger is connected. This way of operation guarantees successful power up procedure with empty battery. In case of empty battery the only power source is the charger. When the battery has been initially charged and the voltage is higher than the PSCLD, N301 switch on voltage the sleep control signal which is connected to the PSCLD for power saving function sleep mode, enters inactive state, high, to enable the regulator that controls the power supply to the VCO to be started. The ASIC, D151 which normally controls the sleep control line has the sleep output inactive, low as long as the system reset, PURX is active, low, from PSCLD. After a delay of about 5–10 ms the system

reset output PURX from PSCLD enters high state. This delay is to ensure that the clock is stable when the ASIC exits reset. The sleep control output from the PSCLD that has been driving an output until now, returns the control to the sleep signal from the ASIC as the PURX signal goes inactive. When the PURX signal goes inactive, high, the charge detection output at PSCLD, that is in input mode when PURX is active, switches to output and goes high indicating that a charger is present. When the system reset, PURX, goes high the sleep control line is forced inactive, high, by the ASIC, D151 via PSCLD, N301.

Once the system has exited reset the battery is initially charged until the MCU writes a new value to the PWM in PSCLD. If the watchdog is not acknowledged the battery charging is switched off when the PSCLD shuts off the power to the baseband. The PSCLD will not enter the power on mode again until the charger has been extracted and inserted again or the power switch has been pressed. The battery is charged as long as the power on line, PWRONX is active low. This is done to allow the phone to be started manually from the power button with the charger inserted not having to extract the charger to get a power up if the battery is empty.

Power On Reset Operation

The system power up reset is generated by the regulator IC, N301. The reset is connected to the ASIC, D151 that is put into reset whenever the reset signal, PURX is low. The ASIC, D151 then resets the DSP, D152 the MCU, D150 and the digital parts in N450. When reset is removed the clock supplied to the ASIC, D151 is enabled inside the ASIC. At this point the 32 kHz oscillator signal is not enabled inside the ASIC, since the oscillator is still in the startup phase. To start up the block requiring 32 kHz clock the MCU must enable the 32 kHz clock. The MCU reset counter is now started and the MCU reset is still kept active, low. 6.5 MHz clock is started to MCU in order to put the MCU, D150 into reset, MCU is a synchronous reset device and needs clock to reset. The reset to MCU is put inactive after 128 MCU clock cycles and MCU is started.

DSP, D152 and N450 reset is kept is kept active when the clock inside the ASIC, D151 is started. 13 MHz clock is started to DSP, D152 and puts it into reset, D152 is a synchronous reset device and requires clock to enter reset. N450 digital parts are reset asynchronously and do not need clock to be supported to enter reset.

As both the MCU, D151 and DSP, D152 are synchronous reset devices all interface signals connected between these devices and ASIC D151 which are used as I/O are set into input mode on the ASIC, D151 side during reset. This avoids bus conflicts to occur before the MCU, D150 and the DSP, D152 are actually reset.

The DSP, D152 and N450 reset signal remains active after that the MCU has exited reset. The MCU writes to the ASIC register to disable the DSP reset. This arrangement allows the MCU to reset the DSP, D152 and N450 when ever needed. The MCU can put DSP into reset by writing the reset active in the ASIC, D151 register

MCU

The baseband uses a Hitachi H3001 type of MCU. This is a 16–bit internal MCU with 8–bit external data bus. The MCU is capable of addressing up to 16 MByte of memory space linearly depending upon the mode of operation. The MCU has a non multiplexed address/data bus which means that memory access can be done using less clock cycles thus improving the performance but also tightening up memory access requirements. The MCU is used in mode 3 which means 8–bit external data bus and 16 Mbyte of address space. The MCU operating frequency is equal to the supplied clock frequency. The MCU has 512 bytes of internal SRAM. The MCU has one serial channel, USART that can operate in synchronous and asynchronous mode. The USART is used in the MBUS implementation. Clock required for the USART is generated by the internal baud rate generator. The MCU has 5 internal timers that can be used for timing generation. Timer TIOCA0 input pin 71 is used for generation of net-free signal from the MBUS receive signal which is connected to the MCU USART receiver input on pin 2.

The MCU contains 4 10–bit A/D converters channels that are used for baseband monitoring. For A/D converter channel usage see section NO TAG.

The MCU, D150 has several programmable I/O ports which can be configured by SW. Port 4 which multiplexed with the LSB part of the data bus is used baseband control. In the mode the MCU is operating this port can be used as an I/O port and not as part of the data bus, D0–D7.

MCU Access and Wait State Generation

The MCU can access external devices in 2 state access or 3 state access. In two state access the MCU uses two clock cycles to access data from the external device In 3 state access the MCU uses 3 clock cycles to access the external device or more if wait states are enabled. The wait state controller can operate in different modes. In this case the programmable wait mode is used. This means that the programmed amount of wait states in the wait control register are inserted when an access is performed to a device located in that area. For area split see NO TAG. The complete address space is divided into 8 areas each area covering 2 MByte of address space. The access type for each area can be set by bits in the access state control register. Further more the wait state function can be enabled separately for each area by the wait state controller enable register.

This means that in 3 state access two types of acccess can be performed with a fixed setting:

– 3 state access without wait states

– 3 state access with the amount of wait states inserted determined by the wait control register

If the wait state controller is not enabled for a 3 state access area no waits states are inserted when accessing that area even if the wait control register contains a value that differs from 0 states.

MCU Flash Loading

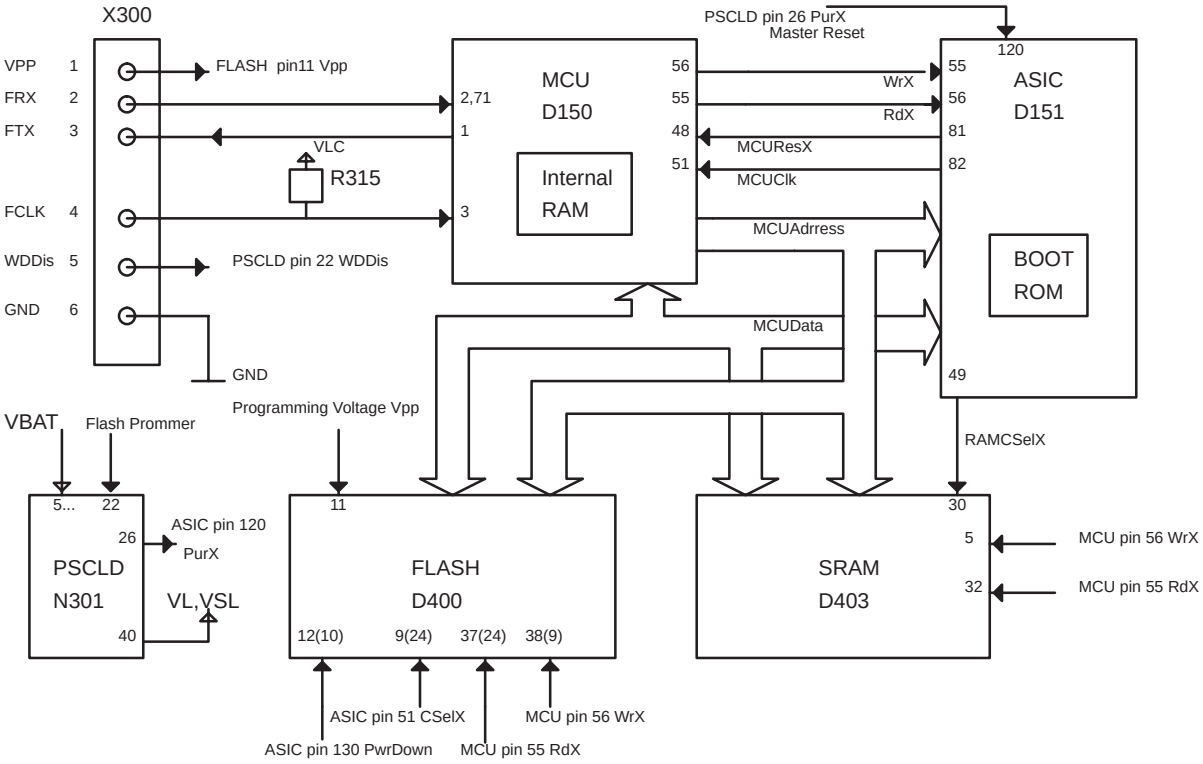
The flash loading equipment is connected to the baseband by means of the test connector before the module is cut out from the frame. Updating SW on a final product is done by removing the battery and connect a special battery that contains the necessary contacting elements. The contacts on the baseband board are test points that are accessable when the battery is detached. The power supply for the base band is supplied via the adapter and controlled by the flash programming equipment. The base band module is powered up when the power is connected to the battery contact pins.

Five signals are required for the flash programming, with the addition of the battery supply. The baseband MCU will automatically wait for flash down loading to be performed if one of the two following criteria are met.

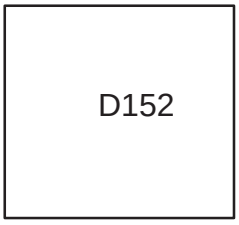
– The flash is found to be empty when tested by the MCU
– The serial clock line at the baseband MCU is forced low when the MCU is exiting reset

The second alternative is used for reprogramming as the flash is not empty in this case. To allow the serial clock line to be forced low during MCU initial boot there is a requirement that the flash prommer can control the power on of the baseband module. This is done by controlling the switching of the battery power supply. This arrangement allows the baseband module to operate in normal mode even if the flash prommer is connected but not active. The flash prommer also disables the power supply watchdog during flash programming to prevent unwanted power off of the baseband. The programming voltage to the flash is applied when the flash prommer has detected that the baseband module is powered. This detection is performed by monitoring the serial interface RX line from the baseband. The RX line is pulled high by a pullup resistor in idle. The VPP voltage is set to 5V as it is not known at this point what type of device is used.

The following diagram shows the block diagram for the baseband flash programming circuitry.



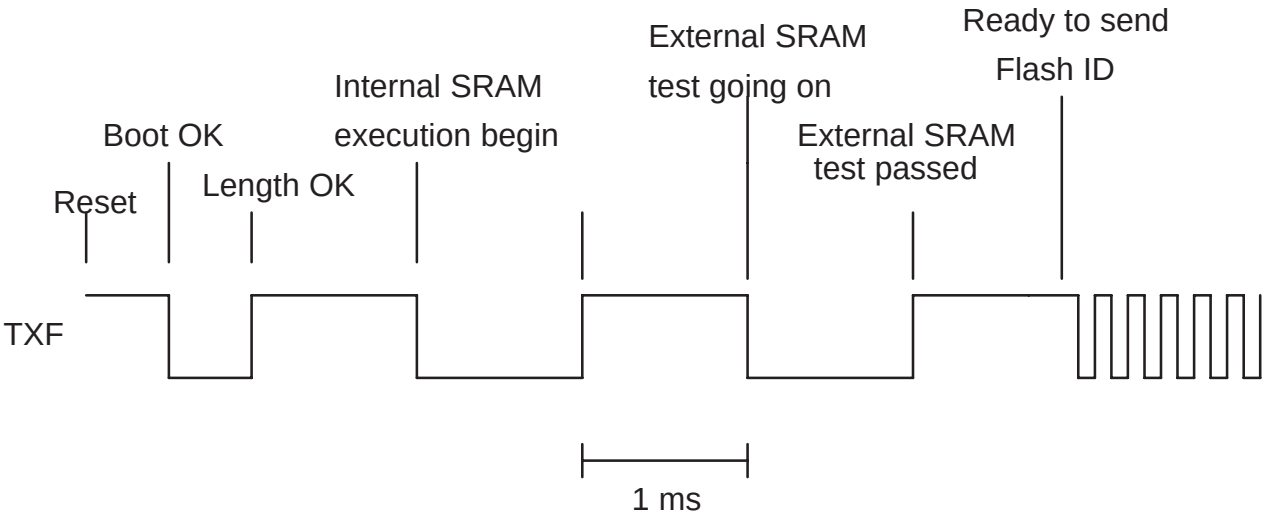
The following picture shows the location of the flash programming contact pads on the PCB. These pads are used for SW updating at after sales locations. A special battery pack is used for this purpose. The battery pack contains contacting elements that can access these pads without having to disassemble the phone.



The interface lines between the flash prommer and the baseband are in low state when power is not connected by the flash prommer. The data transfer between the flash programming equipment and the base band is synchronous and the clock is generated by the flash prommer. The same MCU USART that is used for MBUS communication is used for the serial synchronous communication. The PSCLD watchdog is disabled when the flash loading battery pack and cable is connected.

After the flash battery pack adapter has been mounted or the test connector has been connected to the board the power to the baseband module is connected by the flash prommer or the test equipment. All interface lines are kept low except for the data transmit from the baseband that is in reception mode on the flash prommer side, this signal is called TXF. The MCU boots from ASIC and investigates the status of the synchronous clock line. If the clock input line from the flash prommer is low or no valid SW is located in the flash MCU forces the initially high TXF line low acknowledging to the flash prommer that it is ready to accept data.

The flash prommer sends data length, 2 bytes, on the RXF data line to the baseband. The MCU acknowledges the 2 data byte reception by pulling the TXF line high. The flash prommer now transmits the data on the RXF line to the MCU. The MCU loads the data into the internal SRAM. After having received the transferred data correctly MCU puts the TXF line low and jumps into internal SRAM and starts to execute the code. After a guard time of 1 ms the TXF line is put high by the MCU. After 1 ms the TXF is put low indicating that the external SRAM test is going on. After further 1 ms the TXF is put high indicating that external SRAM test has passed. The MCU performs the flash memory identification based upon the identifiers specified in the Flash Programming Specifications. In case of an empty device, identifier locations shows FFH, the flash device code is read and transmitted to the Flash Prommer.



After that the device mounted on base band has been identified the Flash Prommer down loads the appropriate algorithm to the baseband. The programming algorithm is stored in the external SRAM on the baseband module and after having down loaded the algorithm and data transfer SW, MCU jumps to the external SRAM and starts to execute the code.

The MCU now asks the prommer to connect the flash programming power supply. This SW loads the data to be programmed into the flash and implements the programming algorithm that has been down loaded.

Flash Prommer Connection Using Dummy Battery

For MCU SW updating in the field a special battery adapter can be used to connect to the test points which are accessable through 5 holes in the chassis, located behind the battery. Supply voltage must be connected to this dummy battery as well as the flash programming equipment

Flash, D400

A 4 MBit Boot Block flash is used as the main program memory, D400 the device is 3 V read/program with external 12V VPP for programming. The device has a lockable boot sector. This function is not used since the complete code is reprogrammed. The Boot sector is located at the ”bottom”, definition by Intel, address 00000H–03FFFH. The block is unlocked by a logic high state on pin 12. This logic high level is generated from VPP. The device can be programmed by a VPP of 5V but the programming procedure takes longer. To improve programming the programming voltage used is 12V. The speed of the device is 110 ns although the requirement is 150 ns. The MCU operating at 6.5 MHz will access the flash in 2 state access, requiring 150 ns access time from the memory.

SRAM D402, D403

The baseband is designed to take two different size of SRAMs, 32kx8 and 128kx8, not at the same time. The required speed is 150 ns as the MCU will operate at 6.5 MHz and the SRAM will be accessed in 2 state access. The SRAM has no battery backup which means that the content is lost even during short power supply disconnections. As shown in the memory map the SRAM is not accessable after boot until the MCU has enabled the SRAM access by writing to the ASIC register.

EEPROM D401

The baseband is designed to take an 8kx8 parallel EEPROM. In addition to that a serial 2kx8 device using I2C bus is also designed on the baseband. HD842 will use the 2kx8 serial device over the I2C bus. The I2C bus protocol is implemented in SW and the physical implementation is performed on MCU Port 4.

The parallel device is connected to the MCU data and address bus. The ASIC generates chip select for the EERPROM. To avoid unwanted EEPROM access there is an EERPOM access bit in the ASIC MCU interface. This bit mus be set to allow for EERPOM access. This bit is cleared by default after reset. After each access this bit should be cleared to prevent unwanted EEPROM access. The parallel device used support page mode writing, 64 byte page. One page can be written by the MCU and after that the internal programming procedure is started. The page write operation is internally timed in the device and consecutive bytes must be written within 100 us. During this operation all interrupts must be disabled.

MCU and Peripherals

MCU Port P4 Usage

MCU, D150 port 4 is used for baseband control.

Port Pin	MCU pin	Control Function	Remark
P40	5	Display driver reset	Active low
P41	6		
P42	7		
P43	8		
P44	9	EEPROM SCK	
P45	10	EEPROM SDA	
P46	11	EEPROM write enable	Active low
P47	12	Headset mic amplifier bias	Active loew

Baseband A/D Converter Channels usage in N450 and D150

The auxiliary A/D converter channels inside RFI2, N450 are used by MCU to measure battery voltage. The A/D converters are accessed by the DSP, D152 via the ASIC, D151. The required resolution is 10 bit.

The MCU has 4 10 bit A/D channels which are used for baseband voltage monitoring. The MCU can measure charger voltage, battery size, battery temperature and accessory detection by using it’s own converters.

Baseband N450 A/D Converter Channel Usage

Name:	Usage:	Input volt. range	Remark
Chan 0	Battery voltage	5...9 V	Battery voltage when TX is active
Chan 1	Charger voltage	5...16 V	
Chan 2	Battery size indic.	0...3.2 V	
Chan 3	Battery temperature	0...3.2 V	
Chan 4	System board temp.	0...3.2 V	Not used
Chan 5	Accessory detection	0...3.2 V	
Chan 6		0...3.2 V	Not used
Chan 7	Battery voltage	5...9 V	Battery volt. TX inactive

MCU Baseband A/D Converter Channel Usage

Name:	Usage:	Input volt. range	Remark
Chan 0	Battery temperature	0...3.2 V	
Chan 1	Charger voltage	5...16 V	
Chan 2	Accessory detection	0...3.2 V	
Chan 3	Battery size indicator	0...3.2 V	

Battery Voltage Measurement

The battery voltage is measured using RFI2, N450 A/D converter channel 0 and 7. The converter value supplied from channel 7 is measured when the transmitter is active. This measurement gives the minimum battery voltage. The value from channel 0 is measured when the transmitter is inactive. The battery voltage supplied to the A/D converter input is switched off when the baseband is in power off. The battery voltage measurement voltage is supplied by PSCLD, N301 which performs scaling, the scaling factor is R1(R1+R2), and switch off. The measurement voltage is filtered by a capacitor to achieve an average value that is not depending upon the current consumption behavior of the baseband. To be able to measure the battery voltage during transmission pulse the time constant must be short. The value for the filtering capacitor is set to 1 nF, C319. The scaling factor used to scale the battery voltage must be 1:3, which means that 9V battery voltage will give 3V A/D converter input voltage. The A/D converter value in decimal can be calculated using the following formula:

$A/D = 1023xR1xU_{BAT}/((R1+R2)xU_{ref}) = 1023xU_{BAT}xK$

where K is the scaling factor. $K = R1/((R1+R2)xU_{ref)}$.

Charger Voltage Measurement

The charger voltage is measured to determine the type of charger used. MCU A/D converter channel 1 is used for this purpose. The input circuitry to the charger measurement A/D channel implements an LP–filter. The input voltage must be scaled before it is fed to the A/D converter input. Due to the high input voltage range scaling is performed outside PSCLD, N301. The scaling factor required is 22/(22+100) = 0.18. The charger voltage measurement switch is integrated into PSCLD, N301. Charger voltage is not supplied to the A/D converter input in power off mode. This is done to protect the A/D converter input in case power is switched off and the charger remains connected to the baseband. The charger A/D converter value can be calculated using the same formula as described in above section. The resistor values are different since the scaling factor is larger.

Battery Size Resistor Measurement

The battery size, capacity is determined by measuring the voltage on the BSI pin on the battery pack when the battery is attached to the phone. The MCU A/D converter channel 3 is used for this purpose. The BSI signal is pulled up on the base band using a 47 kohm resistor and the resistor inside the battery pack is reflecting the capacity of the battery. There are two special cases to be detected by the MCU. The first case is the Lithium battery. The Lithium battery has reserved values in the battery size table. Lithium type batteries are all the same from charging point of view. Lithium batteries are charged to a constant voltage and charging is aborted when the predefined voltage is reached. The Lithium battery capacity is a function of the battery voltage. The battery voltage drops linearly as the battery is discharged. The other case that has to be handled is the dummy battery. This battery is used for A/D converter field calibration at service centers and together with a defined voltage on the BTEMP pin on the battery pack to put the baseband into Local mode in production. Battery sizes below 250 mAh will be treated as dummy battery. The different battery size values are shown in tthe table below . The battery size A/D converter value can be calculated using the following formula:

$A/D = RSI/(RSI+47\ k\Omega)x1023$

where RSI is the value of the resistor inside the battery pack.

Battery Size and A/D Converter Value

Battery Type	Battery pack resistor	Capacity	BSI volt.	A/D conv value
Dummy	1 kΩ 2 %	<250 mAh	0.07	21 (83)
Standar battery	6.19 kΩ 2 %	900 mAh	0.37	119 (467)
Extended battery	9.09 kΩ 2 %	1200 mAh	0.52	166 (664)
Slim	3.3 kΩ 2 %	500 mAh	0.21	67 (268)
Lithium	68 kΩ 2 %	400 mAh	1.86	605 (2420)
Lithium	82 kΩ 2 %	8.6 V	2	650 (2601)

Battery Temperatur Measurement

The battery temperature is measured during charging. The BTEMP pin to the battery is pulled up on baseband by a 47 kohm resistor to logic supply voltage, 3.2V. The voltage on the BTEMP pin is a function of the battery pack temperature. Auxiliary A/D channel 3 is used for this purpose. Inside the battery pack there is a 47 kohm NTC resistor to ground. The A/D converter value can be calculated from the following formula:

A/D = RNTC/(RNTC+47 kohm)x1023

where RNTC is the value of the NTC resistor inside the battery pack.

The relation ship between different battery temperature, BTEMP voltage and A/D converter values are shown in following table.

A/D Converter Values for Different Battery Temperatures

Bat. temp.	NTC value	BTEMP voltage	A/D conv. value
Dummy	1 kΩ	0.06 V	21
–25	745.60 kΩ	2.96 V	962
0	164.96 kΩ	2.45 V	796
25	47 kΩ	1.58 V	512
50	16.26 kΩ	0.81 V	263
70	7.78 kΩ	0.45 V	145

Compact HF & Headset Detection

Auxiliary A/D channel 4 is used to detect accessories connected to the system connector using the XMIC. To be able to determine which accessory has been connected MCU measures the DC voltage on the XMIC input. The accessory is detected in accordance with the CAP Accessory specifications. Not all accessories are supported by the HD842 base band that are specified in the CAP Accessory specification.

The base band has a pull–up resistor network of 32 kohm to VA. The accessory has a pull down. The A/D converter value can be calculated using the following formula:

A/D = (ACCI+10 kΩ)/(ACCI+32 kΩ)x1023

where ACCI is the d.c. input impedance of the accessory device connected to the system connector.

The different values for acceptable accessories are given in the following table. The values in below table are calculated using 5 % resistor values and power supply range 3–3.3 V. Due to that the pull up resistor in the XMIC line is divided into two resistors the voltage at the A/D converter input is different from that on the XMIC.

Accessory Detection Voltage

Acc. type	Acc. resistance	Voltage on A/D converter channel 5 (min/typ/max)	A/D converter value(min/max)
Headset	47 kΩ	2.1...2.3...2.45	717...758
Compact HF	22 kΩ	1.7...1.9...2.05	581...631

Keyboard Interface

The keypad matrix is located on a PCB and the interface to the base band is by using connector X101. The electrical specifications are shown in NO TAG. The power on key is also connected to the PSCLD to switch power on. Due to the internal pull up inside PSCLD, N301 to a high voltage, a rectifier, V203 is required in the keypad matrix for the power on keypad to prevent the high voltage to interfere with the keypad matrix.

Series resistors, R261–R264 are implemented in the Column output to reduce the EMI radiation to the UI PCB. Capacitors C257–C260 reduces the EMC radiation and absorbs any ESD produced over an air gap to the keymat. As the serial display driver interface uses ROW5 for data transmission series resistors are needed to prevent keypad or double keypad pressing from interfering with the display communication. In a similar way R265–R269 in the ROW lines reduces the EMI to the UI board. Capacitors C251–C256 implements a LP–filter together with each resistor in the ROW line. The capacitors also absorbs ESD pulses over an air gap to the keymat.

During idle when no keyboard activity is present the MCU sets the column outputs to ”0” and enables the keyboard interrupt. An interrupt is generated when a ROW input is pulled low. Each ROW input on the ASIC, D151 has an internal pull–up. The keyboard interrupt starts up the MCU and the MCU starts the scanning procedure. As there are keypads to be detected outside the matrix the MCU sets all columns to ”1” and reads the ROW inputs if a logic ”0” is read on any ROW this means that one of the 6 possible non matrix keypads has been pressed. If the result was a ”1” on each ROW the MCU writes a ”0” on

each column consecutively while the rest of the column outputs are kept in tri–state to allow dual keypad activation to be detected. After that the keyboard scanning is completed and no activity is found the MCU writes ”0” to all columns, enables the keyboard interrupt and enters sleep mode where the clock to the MCU is stopped. A key press will again start up the MCU.

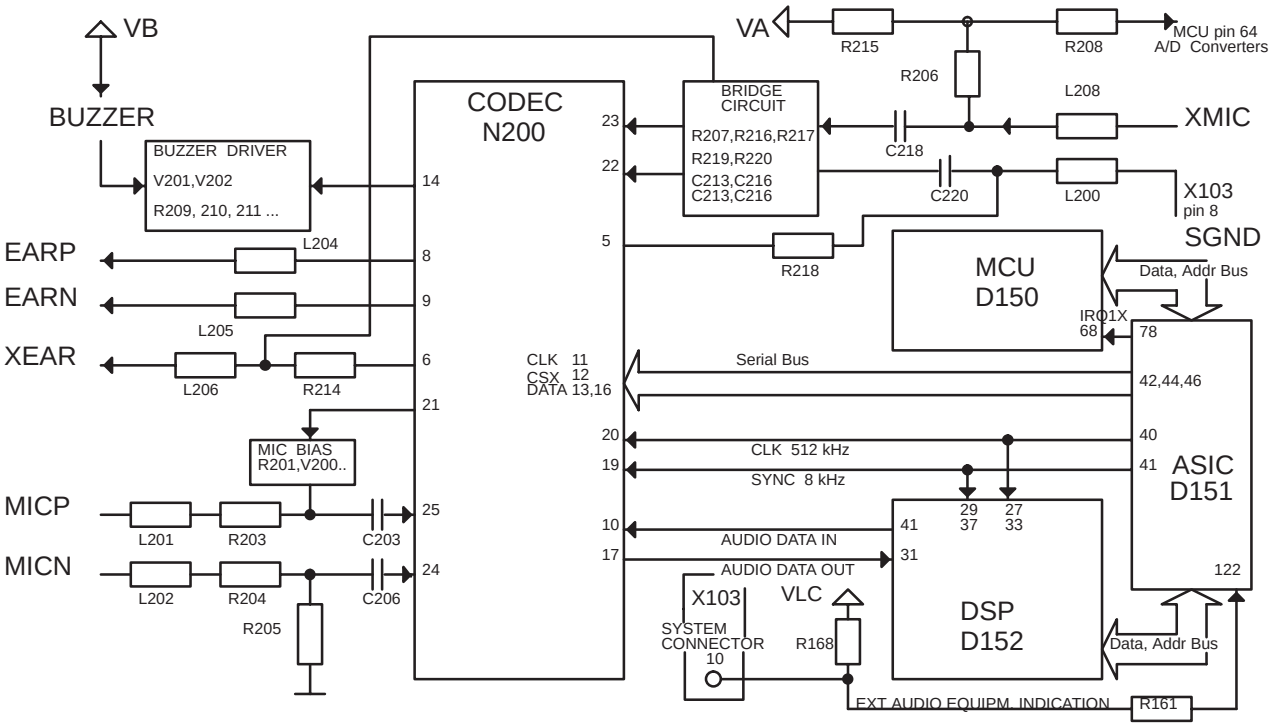
Keyboard and Display Light

The display and keyboard are illuminated by LED’s. The light is normally switched on when a keypad is pressed. The rules for light switching are defined in the SW UI specifications. The display and keyboard light is controlled by the MCU. The LED’s are connected two in series to reduce the power consumption. Due to the amount of LED’s required for the keyboard and display light they are divided into three groups. Each group has it’s own control transistor. The LED switch transistor is connected as a constant current source, which means that the current limiting resistor is put in the emitter circuitry. This arrangement will reduce LED flickering depending upon battery voltage and momentary power consumption of the phone. The LED’s are connected straight to the battery voltage. This connection allows two LED’s to connected in series. The battery voltage varies a lot depending upon if the battery is charged, full or empty. The switching transistor circuitry is designed to improve this as mentioned earlier.

The LED transistor control lines are coming from PSCLD. The MCU controls these lines by writing to PSCLD using the serial control bus. There are two LED control lines provided by the PSCLD. The display light control is connected to a separate control line. The keyboard light control is common to the two transistors. This means that the keyboard and display light can be controlled separately. The advantage of this is that the power dissipation and heating of the phone can be reduced by only having the required lights switched on.

Audio Control

The audio codec N200 is controlled by the MCU, D150. Digital audio is transferred on the CODECB(5:0). PCM data is clock at 512 kHz from the ASIC and the ASIC also generates 8 kHz synchronization signal for the bus. Data is put out on the bus at the rising edge of the clock and read in at the falling edge. Data from the DSP, D152 to the audio codec, N200 is transmitted as a separate signal from data transmitted from the audio codec, N200 to the DSP, D152. The communication is full duplex synchronous. The transmission is started at the falling edge of the synchronization pulse. 16 bits of data is transmitted after each synchronization pulse.



The 512 kHz clock is generated form 13 MHz using a PLL type of approach which means that the output frequency is not 512 kHz at any moment. The frequency varies as the PLL adjusts the frequency. The average frequency is 512 kHz. The clock is not supplied to the codec when it is not needed. The clock is controlled by both MCU and DSP. DTMF tones are generated by the audio codec and for that purposes the 512 kHz clock is needed. The MCU must switch on the clock before the DTMF generation control data is transmitted on the serial control bus.

The serial control bus uses clock, data and chip select to address the device on the bus. This interface is built in to the ASIC and the MCU writes the destination and data to the ASIC registers. The serial communication is then initiated by the ASIC. Data can be read form the audio codec, N200 via this bus.

Internal Audio

The bias for the internal microphone is generated from the PSCLD, N301 analog output, VA using a bias generator. The bias generation is designed in such a way that common mode signals induced into the microphone capsule wires are suppressed by the input amplifier in the audio codec. The bias generator is controlled by the MCU to save power, the control signal is taken from the audio codec, N200 output latch, pin 21, when the microphone is not used, in idle the bias generator is switched off. The microphone amplifier gain is set by the MCU to match with the used microphone, 35 dB. The microphone amplifier input to the audio codec is a symmetrical input.

The microphone signal is connected to the baseband using filtering to prevent EMC radiation and RF PA signal to interfere with the microphone signal. L201

and C201 forms the first part of this filter. R203 and C202 forms the second part of this filter. A similar filter is used in the negative signal path of the microphone signal. R205 is connected in the ground path for the microphone bias current. R202 supplies the bias current to the microphone from the generator circuitry R201, C200 and V200. A transient suppressor, V204, is connected across the microphone terminals to protect the microphone against ESD.

The earpiece amplifier used for the internal earpiece is of differential type and is designed as a bridge amplifier to give the output swing for the required sound pressure. Since the power supply is only 3V a dynamic type ear piece has to be used to achieve the sound pressure. This means that the ear piece is a low impedance type and represents a significant load to the output amplifier. Series inductors are implemented to prevent EMC radiation from the connection on baseband to the earpiece. The same filter also prevents the PA RF field from causing interference in the audio codec, N200 output stage to the earpiece.

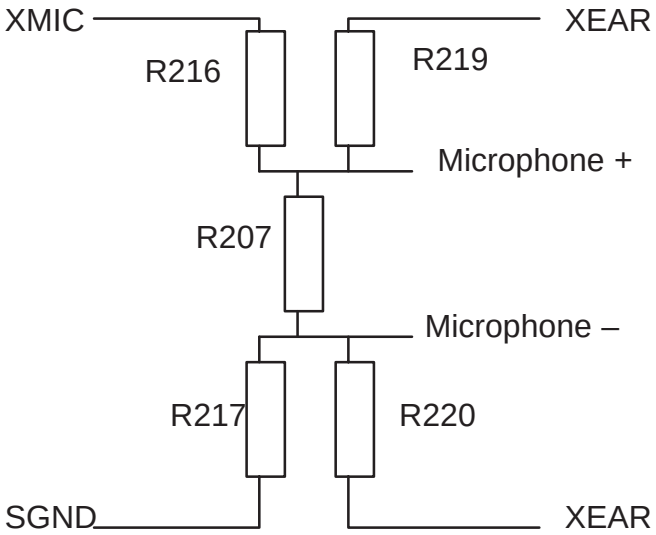
The buzzer is controlled by the PWM output provided by the audio codec, N200. Transistors V201 and V202 acts as amplifier and, impedance conversion for the low impedance buzzer. The buzzer is driven directly from the battery voltage. As the buzzer is connected to the baseband via the keyboard the battery voltage provided by VBKEY and the buzzer driving signal BUZZER are EMC protected. As the buzzer is a dynamic one the impedance shows a clear inductance. Therefore a free running diode V203 is used to clip the voltage spikes induced in the buzzer line when the buzzer is switched off.

The buzzer frequency is determined by the internal setup of N200. The frequency is determined by the MCU via the serial control bus. The output level can be adjusted by the PWM function which is attached to the buzzer output in N200.

External Audio

The external microphone audio signal is applied to the baseband system connector and connected to the audio block using signals XMIC and SGND. In order to improve the external audio performance the input circuitry is arranged in a sort of dual ended. A wheatstone type of bridge configuration is created by resistors R216, R217, R219 and R220. The signal is attenuated around 20 dB to not cause distortion in the microphone amplifier. The microphone signal is attenuated by resistors R216, R207 and R217. Two allow the external earpiece to be driven dual ended the external microphone signal ground is connected to the negative output of the external audio earpiece amplifier. This means that with reference to audio codec, N200 ground there is a signal level on the SGND line. This arrangement requires that the external microphone amplifier supplies the signal on the SGND line to the XMIC line. With this arrangement the differential voltage over R207 caused by the signal in the SGND line is canceled. There is however a common mode component which is relatively high presented at both the external microphone input pins at the audio codec input, pins 22 and 23. The microphone amplifier has a good common mode rejection ratio but a slight phase shift in the signals will remove the balance. To compensate

for this the signal from the external earpiece amplifier positive output, which also feeds the external audio output from the baseband is feed to the remaining resistors in the bridge, R219 and R220. This arrangement will attenuate the common mode signal presented to the microphone amplifier caused by the audio signal in the SGND line. Since the positive output from the audio codec, XEAR signal introduces a DC signal to the microphone amplifier the DC signal on the XMIC and SGND lines are blocked by capacitors C218 and C220.



The external audio output is the XEAR signal on the system connector pin. The XEAR signal is taken from audio codec N200 pin 6. The output impedance is increased to 32 ohms by resistors R222 and R214. This resistors prevents the output amplifier from being short circuited even if the pin at the system connector is short circuited. An ESD capacitor, C225, is connected to ground at the connection point of R222 and R214. R222 is added to N200 pin 6 output as the output amplifier can not be loaded directly with the ESD capacitor. The DC voltage at the XEAR output is used to control the mute function of the accessory. When internal audio is selected the XEAR amplifier in N200 is switched off and the DC voltage at the output on pin 5 is removed. External audio output level is adjusted by the variable gain amplifier in the N200 by MCU via the serial control bus from the ASIC, D151. L206 and C 214 is EMC protection for the XEAR signal at the system connector. This filter also prevents RF signals induced in the external cables from creating interference in the audio codec output stage.

DSP

The DSP used in NHE–5 is the TI 320C541. This is a 16 bit DSP that can use external and/or internal memory access. The DSP can operate in two modes microprocessor mode or microcontroller mode. The difference between the two modes are that in microprocessor mode the DSP boots from external memory while in the microcontroller mode the DSP boots from internal ROM. The DSP external memory access is devided into data, program and I/O access. The type of access is indicated on three control pins that can be used for memory control.

The DSP, D152 executes code from the internal ROM. The baseband also provides external memories for the DSP, D410, D411. The DSP is capable of addressing 64 kword of memory. The memory area is divided into a code execution area and a data storage area. The code execution area is located at address 8000H–FFFFH in the internal ROM. The external memories are arranged in such a way that the DSP can access the external memories both as data storage and code execution. The memory chip select is taken from the memory access strobe signal from the DSP. This means that the memory is active during any memory access. The SRAMs are configured in chip select controlled write mode. This means that both the write signal and the output enable signal are active at the same time, and the actual write occours at the rising edge of the chip select signal. This implementation is required since the DSP supports only one signal for write/read control.The DSP, D152 executes code from the internal ROM. The baseband also provides external memories for the DSP, D410, D411. The DSP is capable of addressing 64 kword of memory. The memory area is divided into a code execution area and a data storage area. The code execution area is located at address 8000H–FFFFH in the internal ROM. The external memories are arranged in such a way that the DSP can access the external memories both as data storage and code execution. The memory chip select is taken from the memory access strobe signal from the DSP. This means that the memory is active during any memory access. The memories are connected in such a way that the write control is CE controlled write. This means that both the write signal and the output enable signal are active at the same time. This implementation is required since the DSP supports only one signal for write/read control.

The DSP is operating from the 13 MHz clock. In order to get the required performance the frequency is internally increased by a PLL by a factor of 3. The PLL requires a settling time of 50 us after that the clock has been supplied before proper operation is established. This settling counter is inside the DSP although the ASIC, D151 contains a counter that will delay the interrupt with a programmable amount of clock cycles before the interrupt causing the clock to be switched on is presented to the DSP. The DSP has full control over the clock supplied to it. When the DSP is to enter the sleep mode the clock is switched off by setting a bit in the ASIC register. The clock is automatically switched on when an interrupt is generated.

The DSP also has two synchronous serial channels for communication. One channel is used for data transmission between the DSP and the audio codec. This channel is operating at 512 kbits and clock and synchronization signal is provided by the ASIC, D151. The other channel is used for debugging purposes and uses the same clock and synchronization signals. The DSP has an interrupt controller servicing four interrupts and one non maskable interrupt, NMI. The interrupts have fixed priority which can only be changed by changing the interconnection between the interrupt sources by HW.

The ASIC contains DSP support functions as modulator,encryption/decryption using algorithms A5/A51, RF power ramp generation/AGC control, AFC control, Synthesiser serial interface, frame counters, timer, RFI2 interface, RX and TX

power control timing. RF power ramp timing/AGC control, AFC control, synthesiser control are timed to the value of the frame counter. This means that data is loaded into the registers and transferred when the frame counter and the reference value matches. This allows timing of synthesiser control power ramp and start of TX data to be controlled very precisely.

As the receiver and the transmitter is not operating at the same time the TX power ramp function is used to control the AGC in the receiver during the reception. This requires the DSP to continously modify the values in the TX ramp SRAM to fit the ramp during TX and the AGC value during reception.

DSP ASIC Access

The DSP is accessing the ASIC in the DSP I/O area. 2 wait states are required for the ASIC access. Some of the DSP registers located in the ASIC are retimed to the internal ASIC clock and requires special handling with respect to consecutive writing. This means that the same register can not be written again until a specified time has passed. To cope with this DSP is inserting NOP instructions to satisfy this requirement.

DSP Interrupts

The DSP supports 4 external interrupts. Three interrupts are used. The ASIC, D151 generates two of the interrupts. One interrupt is generated by RFI2, N450 auxiliary A/D converter. This interrupt is generated when a baseband measurement A/D conversion is completed. The interrupts to the DSP are active low.

INT0 which is the highest priority interrupt is used for data reception from the receiver and is generated by the ASIC. INT1 signal is used for auxiliary A/D channel conversions generated by the RFI2. This interrupt is generated by RFI2 and is a result of measurement requests from the DSP. There are 8 auxiliary channels supported by the RFI2, not all are used in HD842 even if most of the channels are connected. INT3 is a low priority interrupt generated by the ASIC timer. The DSP programs the timer value and an interrupt is given when the timer expires. The interrupt must be active at least 1 ??? DSP clock cycle as it is sampled on the rising/falling edge by the DSP. All interrupts are active low.

INT0 is used for the reveiver A/D converter in RFI2. The ASIC reads the data from the receiver path A/D converter in RFI2 at every data available signal activation from the RFI2. After the data transfer when the data is stored in the ASIC the ASIC generates a receiver interrupt to the DSP using INT1 signal. The DSP enters the interrupt routine and services the interrupt and reads the data from the ASIC.

INT1 signal is used for the auxiliary A/D converter channels in RFI2. These A/D channles are used for baseband battery voltage monitoring. Two channels are used for battery monitoring. The start of the A/D conversion task is timed in such a way that auxiliary channel 1 results are measured during transmission whne the PA is active and channel 8 is measuring when the PA is off.

Unused interrupt controller inputs are tied high.

DSP Serial Communications Interface

The DSP contains two synchronous serial communications interface. One of the interfaces are used to communicate with the audio codec, N200. The 512 kHz clock required for the data transfer is provided by D151 as well as the 8 kHz synchronization signal. Data is transferred on to lines, RX and TX creating a full duplex connection. Data is presented on the bus on the first rising edge of the clock after the falling edge of the synchronization pulse. Data is read in by each device on the falling edge of the clock. Data transfer is 16 bits after each synchronization pulse.

The DSP, D152 has control over the clock provided to the audio codec. The DSP can switch on the clock to start the communication and switch it off when it is not needed. This clock is also under control of MCU, D150.

RF Synthesizer Control

The synthesizer control is performed by the DSP, D152 using the ASIC, D151 as the interfacing and timing device. Different synthesizer interface are supported and the required interafce can be selected by the DSP at the initialisation stage of the ASIC. The synthesizer interface also includes timing registers for programming synthesizer data. The DSP loads the synthesizer data into the transmission registers in the ASIC synthesizer interface together with the timing information. The system timing information is used for synthesizer data loading. When the system timing register, frame counter, value matches with the timing value programmed into the synthesizer interface the interface transmits the loaded data to the RF synthesizer and the VCO frequency is changed accordingly. As the synthesizer may be powered off when not needed the interface pins towards the synthesizer can be put in tri–state or forced low when the interface is not active.

RFI2, N450 Operation

The RFI2, N450 contains the A/D and D/A converters to perform the A/D conversion from the received signal and the D/A converters to perform the conversion for the modulated signal to be supplied to the transmitter section. In addition to this the RFI2 chip also contains the D/A converter for providing AFC voltage to the RF section. This AFC voltage controls the frequency of the 13 MHz VCXO which supplies the system clock to the baseband. The RFI2, N450 also contains the D/A converter to control the RF transmitter power control. The power control values are stored in the ASIC, D151 and at the start of each transmission the values are read from the ASIC, D151 to the D/A converter producing the power control pulse. This D/A converter is used during the reception to provide AGC for the receiver RF parts.

The RFI2 contains the interface between the baseband and the RF. RFI2 circuit contains the A/D converters required for the receiver and the D/A converters

required for the transmission. In addition to this the RFI2 contains a 10 bit D/A convereter for AFC control and one of the receiver A/D converters has a multiplexed input for 8 additional channels used for baseband monitoring functions. The A/D converters are 12 bit sigma delta type. This means that the digital output is centered around the reference voltage and the output value is both negative and positive. The RFI2 has an internal reference voltage for the A/D and D/A converters that can be switched off to save power. The reference has external filtering capacitors to improve the converter performance. The transmitter D/A converters are followed by interpolator and post filter. The filter is of switch capacitor type and the filter parameters are taken into account when modulator parameters are calculated. The AFC D/A converter is static and requires no clock for operation. This means that the RFI2 clock can be switched off and the AFC value will be kept.

One of the A/D converters used for receiver signal conversion can be used as an auxiliary converter that supplies 8 channels for baseband measurement purposes. When the converter is used in this mode each conversion generates an interrupt directly to the DSP. The DSP operates this converter via the ASIC, D151.

Data communication between the ASIC, D151 and RFI2, N450 is carried out on a 12 bit parallel data bus. The ASIC, D151 uses 4 address lines to access RFI2, N450. Depending on the direction of the communication either the write control signal is used to write data to RFI2, N450 or the read signal is used to read data from RFI2, N450. The ASIC, D151 supplies 13 MHz clock to the RFI2, N450. This clock is used as reference for the A/D and D/A converters. Communication between the ASIC, D151 and the RFI2, N450 is related to the clock.

The signal from the RF receiver is attenuated at the RFI2 converter input. R454 forms together with the output impedance from the receiver section an attenuator for the input signal to N450. This attenuator is symmetric as it is connected between the two input signals, improving the S/N compared to an attenuator towards ground.The attenuation is done in a symmetric way by series resistors and a resistor between the two inputs. The benefit of this is that the attenuator ground noise is removed and the bias voltage error between the two inputs are reduced. This also affects the settling time in case the analogue supply to RFI2 is switched off. The settling time is reduced due to this attenuator.

The auxiliary channels supported by the RFI2 uses one of the receiver A/D converters as the A/D converter. Due to the type of converter used for the receiver converters the value read from the auxiliary channels can be negative. The input voltage applied to the auxiliary channels must be within 0.5–3.0 V. A 12 bit value is received from the auxiliary channel measurement. The auxiliary channel conversion complete is sent direct to the DSP as an interrupt, INT1. The DSP reads the value using direct access through the ASIC to the RFI2 converter. The conversion is started by the DSP writing the address of the channel to be measured to the ASIC register. The ASIC then writes the selected channel to RFI2 and the conversion is started. The DSP may sample the same channel for more than one value as the A/D converter will produce conti-

nuosly new values. Several samples may be used for example in battery voltage measurement to calculate an avarage value from the results.

The RFI2, N450 digital supply is taken from the baseband main digital supply. The analog power supply, 4.5V is generated by a regulator supplied from the RF section. The external transistor required for the regulator is provided by the baseband, V450. The analog power supply is always supplied as long as the baseband is powered, if R342 is assembled. The RFI2, N450 analog power supply can be switched off during sleep by removing R342 and adding R349. In this case the RFI2, N450 analog power supply is in the control of the PSCLD, N301 sleep control signal.

Receiver Timing and AGC

RF receiver power on timing is performed by the ASIC, D151. The DSP, D152, can program the time when the receiver is to be powered on. The timing information is taken from the system timing that is based upon the frame counter inside the ASIC, D151 which is synchronised to the base station carrier frequency using AFC to tune the receiver. As transmission and reception takes place at different time the D/A converter used for transmitter power control is used to control the AGC of the receiver during reception. This requires the DSP, D152 to alter the content of the SRAM containing the information that is written to the D/A converter for the reception and the transmission.

RF Transmitter Timing and Power Control

The RF Power Amplifier (PA) timing control is performed by the ASIC, D151. The power control is performed by the ASIC D151 using the D/A converter in N450. The ASIC, D151 controls the power supply voltage to the RF transmitter sections. As the first step the relevant circuits are powered on using the TX power control output from the ASIC, D151. The timing for powering on the TX circuits is generated from the ASIC internal system timing circuitry, frame counter. As the RF TX circuitry needs time to stabilize after power on before the actual transmitter can be started there is a programmable delay before the ASIC, D151 starts to write the power ramp data to the D/A converter inside N450. The TXC signal which is generated in this way controls the power ramp of the PA and the power level for that burst. At the end of the burst the power ramp is written to the D/A converter inside N450. The data that creates the power ramp and final power level is stored in a SRAM inside the ASIC, D151. At the start of the ramp the contents of the SRAM is read out in increasing address order. At the end of the ramp the contents is read out in decreasing adress order. The power level during the burst is determined by the last value in the SRAM, this value is the value that will remain in the D/A converter during the burst. The DSP, D152 may change the shape of the falling slope of the poer ramp by writing new values to the power ramp SRAM during the burst.

As the transmitter may have to adjust the transmitter burst due to the distance from the base station there is an additional timer for this purpose. This timing is

called the timing advance and will cause the transmission to start earlier when the distance to the base station increases.

SIM Interface

The SIM interface is the serial interface between the smart card and the base-band. The SIM interface logic levels are 5V since no 3V technology SIM is yet available. The baseband is designed in such a way that a 3V technology SIM can be used whenever it is available. The SIM interface signals are generated inside the ASIC. The signals coming from the ASIC are converted to 5V levels. The PSCLD circuit is used as the logic voltage conversion circuit for the SIM interface. The PSCLD circuit also contains the voltage regulator for the SIM power supply. The control signals from the ASIC to PSCLD are at 3V level and the signals between PSCLD and the SIM are 5V levels. An additional control line between the ASIC and the PSCLD is used to control the direction of the DATA buffer between the SIM and the PSCLD. In a 3V technology environment this signal is internal to the ASIC only. The pull up resistor required on the SIM DATA line is integrated into the PSCLD and the pull–up is connected to the SIM regulator output inside PSCLD. In idle the DATA line is kept as input by both the SIM and the interface on the base band. The pull–up resistor is keeping the DATA line in it's high state.

The power up and power down sequences of the SIM interface is performed according to ISO 7816–3. To protect the card from damage when the power supply is removed during power on there is a control signal, CARDIN, that automatically starts the power down sequence. The CARDIN information is taken from the battery size indicator signal, BSI, from the battery connector. The battery connector is designed in such a way that the BSI signal contact is disconnected first, while the power is still supplied by the battery, and the battery power contacts are disconnected after that the battery pack has moved a specified distance.

Since the power supply to the SIM is derived from PSCLD also using 3V technology SIM the power supply voltage of the SIM regulator is programmable 3.15/4.8 V. The voltage is selected by using the serial control bus to PSCLD. The default value is set to 3.2V nominal.

For cross compatibility reasons the interface should always be started up using 5V. The 3V technology SIM will operate at 5V but a 5V SIM will not operate at 3V. The supply voltage is switched to 3V if the SIM can accept that. The SIM has a bit set in a data field indicating it's capability of 3V operation.

The regulator control signal is derived from the ASIC and this signal controls the operation of the SIM power supply regulator inside PSCLD. To ensure that the powered off ASIC doesn't cause any uncontrolled operations at the SIM interface the PSCLD signals to the SIM are forced low when the PURX signal is active, low. This implementation will ensure that the SIM interface can not be activated by any external signal when PSCLD has PURX active. When PURX goes inactive the control of the interface signals are given back to the ASIC signals controlling PSCLD SIM interface operations.

The clock to the SIM can be switched off if the SIM card allows stopping of the clock. The clock can be stopped either in high or low state, determined by the card data. For cards not allowing the clock to be stopped there is a 1.083 MHz clock frequency that can be used to reduce the power consumption while the clock is running. In this case the VCO must be running all the time. When the clock is stopped and the status of the CARDIN signal changes, battery is removed, the clock to the SIM is restarted inside the ASIC and the SIM power down sequence is performed.

To be able to handle current spikes as specified in the SIM interface specifications the SIM regulator output from PSCLD must have a ceramic capacitor of 100 nF connected between the output and ground close to the SIM interface connector. To be able to cope with the fall time requirements and the disconnected contact measurements in type approval the regulator output must be actively pulled down when the regulator is switched off. This active pull–down must work as long as the external battery is connected and the battery voltage is above the PSCLD reset level.

The SIM power on procedure is controlled by the MCU. The MCU can power up the SIM only if the CARDIN signal is in the inactive state, low. Once the power up procedure has been started the ASIC takes care of that the power up procedure is performed according to ISO 7816–3.

The SIM interface uses two clock frequencies 3.25 MHz or 1.625 MHz during SIM communication. The data transfer speed in the SIM GSM session is specified to be the supplied clock frequency/372. The ASIC SIM interface supplies all the required clock frequencies as well as the required clock frequency for the UART used in the SIM interface data transmission/reception.

SIM Interface and Support in D151

The signal from the BSI input from the battery is fed to D151, pin 25. This pin has a special input cell that has specific input levels to convert the BSI signal into the card detection logical control signal for the SIM interface in the ASIC. When the input voltage has been low, less than 1.5V the output from the cell will remain low until the input voltage exceeds 2.3V. If the input voltage has been more than 2.8V the input will remain high until the input voltage has decreased to at least 1.9V. For all specified battery types the BSI voltage will stay below 2.3V. If the voltage on this pin exceeds 2.3V the card detection signal will be active and the card will be powered down. It is not possible to power up the card as long as the card detection signal is active, high.

BART ASIC

Display Driver Interface

The display driver used is Seiko SD1232. The display driver has internal voltage triple circuitry for LCD voltage generation. Capacitors C266 and C267 are used in the voltage converter. Capacitor C 268 is the filtering capacitor for the

voltage generator output. Capacitors C261–C264 are filtering capacitors for the supply voltage to the display driver back plane voltages. Resistor network R271 and R272 forms the feedback network for setting the contrast for the display.

The HD842 Base Band uses a serial interface to the Seiko LCD driver. The serial interface is designed in the ASIC. The MCU writes data into the serial interface in the ASIC and it is then transmitted to the LCD driver. The LCD driver reset is controlled by the MCU on P40. The display driver reset is dual edge active. The P40 pin on the MCU has a pull down resistor, R166 to ensure that the LCD driver reset is low at power up. After exiting reset one of the first tasks for the MCU is to set the P40 to output and low, ”0”. After at least 100 us the reset signal to the display driver is taken high, ”1”. This rising edge reset selects 80XX type MCU interface. The serial interface setting of the driver will override this. After resetting the display driver the MCU starts the initialization procedure using the serial interface in the ASIC, D151.

Communication with the serial driver takes place on the LCDSIOCONB(5:0). The display driver requires serial data, serial clock and command/display information during the serial transfer. The display driver has it’s own chip select which is active during the transfer, there are other devices on the same serial bus as well. The command/display information is transmitted on the keyboard ROW5 output. Due to the fact that the keyboard interface is used during display driver transfers the keyboard activities must be disabled during display driver communication. This means that the column output from the ASIC must be put in high impedance state not to interfere with the data transmission if keypads are pressed.

The timing required for the serial interface is provided by the ASIC and the operation of ROW5 depends upon the display driver interface initialization. For the serial interface it is used for command/display data control. The serial clock is 541 kHz.

The clock to the display driver interface in the ASIC is automatically switched on when a write operation to the interface has taken place. The MCU can force the clock to be continuously on by writing the clock on to the CTSI block. The default assumption is that the MCU forces the clock to be continuously on only when a large amount of data is to be transmitted, such as segment test at power up.

RF Block

Introduction

The RF module carries out all the RF functions of the transceiver. This module works in the GSM system.

Components are located on both sides of the PWB. All components with height more than 2 mm are on side two and lower than 2 mm components are on both sides of PWB.

EMC leakage is prevented with magnesium shields. Shields conducts also heat out of the inner parts of the phone thus preventing excessive temperature rise.

Receiver

The receiver is a double conversion receiver.

The received RF signal from the antenna is fed via a duplex filter to the receiver unit. The signal is amplified by a discrete low noise preamplifier. The gain of the amplifier is controlled by the AGC control line (PDATA0). The nominal gain of 16.5 dB is reduced in the strong field condition about 36 dB. After the preamplifier the signal is filtered by SAW RF filter. The filter rejects spurious signals coming from the antenna and spurious emissions coming from the receiver unit.

In GSM systems the filtered RF–signal is down converted by the passive diode mixer. The first IF frequency is 71 MHz in GSM. The first local signal is generated by the UHF synthesizer. The IF signals 71 MHz is amplified and filtered by SAW filter in GSM. The filter rejects adjacent channel signal, intermodulating signals and the last IF image signal.

The filtered IF signal is fed to the receiver part of the integrated RF circuit CRFRT. In CRFRT the filtered IF signal is amplified by an AGC amplifier which has gain control range of 57 dB. The gain is controlled by an analog signal via TXC line. The amplified IF signal is down converted to the last IF in the mixer of CRFRT. The last local signal is generated from VHF VCO by dividing the original signal by 4 in the dividers of CRFRT.

The last IF frequency is 13 MHz. The last IF is filtered by a ceramic filter. The filter rejects signals of the adjacent channels. The filtered last IF is fed back to CRFRT where it is amplified and fed out to RFI via RXINN and RXINP lines.

Duplex Filter

The duplex filter consists of two functional parts; RX and TX filters. The TX filter rejects the noise power in the RX frequency band and TX harmonic signals. The RX filter rejects blocking and spurious signals coming from the antenna.

Pre–Amplifier

The bipolar pre–amplifier amplifies the received signal coming from the antenna. In the strong field conditions the gain of the amplifier is reduced 36 dB in GSM, typically.

Parameter	*Value*
Frequency band:	*935–960 Mhz*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Current consumption (min/typ/max):	*5...6....7 mA*
Insertion gain (min/typ/max):	*15...16.5...17 dB*
Gain flatness:	*±0.5 dB*
Noise figure (typ/max):	*2.0...2.5 dB*
Reverse isolation (min):	*15 dB*
Gain reduction (min/typ/max):	*33...36...39 dB*
IIP3: (min/typ):	*–12...–10 dBm*
Input VSWR; zo=50 Ω (max):	*2.0*
Output VSWR; zo=50 Ω (max):	*2.0*

RF Interstage Filter

The RX interstage filter is a SAW filter in GSM. The filter rejects spurious and blocking signals coming from the antenna. It rejects the local oscillator signal leakage, too.

First Mixer

The first mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer down converts the received RF signal to IF signal.

Parameter	*Value*
RX frequency range:	*935–960 Mhz*
LO frequency range:	*1006–1031 Mhz*
IF frequency:	*71 Mhz*
Conversion loss (min/typ/max):	*5...6...7 dB*
IIP3 (min/typ):	*2...5 dBm*
LO – RF isolation (min):	*15.0 dB*
LO power level (min):	*3 dBm*

First IF Amplifier

The first IF amplifier is a bipolar transistor amplifier.

Parameter	*Value*
Operation frequency:	*71 Mhz*
Supply voltage (min/typ/max):	*4.27...4.5...4.73*
Current consumption (typ/max):	*12...15 mA*
Insertion gain (min/typ/max):	*18...20...22 dB*
Noise figure (typ/max):	*3.5...4.0 dB*
IIP3 (min/typ):	*–5...–3 dBm*

First IF Filter

In GSM the first IF filter is a SAW filter. The IF filter rejects some spurious and blocking signals coming from the front end of the receiver.

Receiver IF Circuit, RX part of CRFRT

The receiver part of CRFRT consists of an AGC amplifier of 57 dB gain, a mixer and a buffer amplifier for the last IF. The mixer of the circuit down converts the received signal to the last IF frequency. After external filtering the signal is amplified and fed to baseband circuitry. The supply current can be switched OFF by an internal switch, when the RX is OFF.

Parameter	*Value*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Current consumption (max):	*35 mA*
Input frequency range (min/max):	*45 MHz (–1 db point) ...87 MHz (–3 dB point)*
Local frequency range of mixer (min/max):	*42.5...100 MHz*
2nd IF range (min/max):	*2...17 MHz*
Voltage gain (max gain) of AGC amlifier (min):	*47 dB*
Noise figure (max):	*15 max gain*
AGC gain control slope (min/typ/max):	*40...84...100 dB/V*
Mixer output 1 dB compression point (typ):	*1.0 V_{PP}*
Gain of the last IF buffer:	*30*
Max output level after last IF buffer (typ):	*1.6 V_{PP}*

Last IF Filter

The last IF is 13 MHz. The ceramic filter on last IF makes part of the channel selectivity of the receiver.

Transmitter

The TX intermediate frequency is modulated by an I/Q modulator contained on transmitter section of CRFRT IC. The TX I and Q signals are generated in the RFI interface circuit and they are fed differentially to the modulator.

Modulated intermediate signal is amplified or attenuated in temperature compensated controlled gain amplifier (TCGA). The output of the TCGA is amplified and the output level is typically –10 dBm.

The output signal from CRFRT is band–pass filtered to reduce harmonics and the final TX signal is achieved by mixing the UHF VCO signal and the modulated TX intermediate signal with passive mixer. After mixing the TX signal is

amplified and filtered by amplifier and filters. These filters are dielectric filters. After these stages the level of the signal is typically 1 mW (0 dBm) in GSM.

The discrete power amplifier amplifies the TX signal to the desired power level. The maximum output level is typically 0.8...2.0 W.

The power control loop controls the output level of the power amplifier. The power detector consists of a directional coupler and a diode rectifier. Transmitted power is controlled with controlled gain amplifier (TCGA) on TX path of CRFRT. Power is controlled with TXC and TXP signals. The power control signal (TXC), which has a raised cosine form, comes from the RF interface circuit, RFI.

Modulator Circuit, TX part of CRFRT

The modulator is a quadrature modulator contained in TX section of CRFRT IC. The I and Q inputs generated by RFI interface are d.c. coupled and fed via buffers to the modulator. The local signal is divided by two to get accurate 90 degrees phase shifted signals to the I/Q mixers. After mixing the signals are combined and amplified with temperature compensated controlled gain amplifier (TCGA). Gain is controlled with power control signal (TXC). The output of the TCGA is amplified and the maximum output level is –10 dBm, typically.

Parameter	*Value*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Supply current (max):	*35 mA*

Transmit frequency input	*Value*
LO input frequency (min/max):	*170...400 MHz*
LO input power level (typ):	*0.2 V_{PP}*
LO input resistance (min/typ/max):	*70...100...130 Ω*
LO input capacitance (typ):	*4 pF*

Modulator Inputs (I/Q):	*Value*
Input bias current, balanced (max):	*100 nA*
Input common mode voltage (min/typ/max):	*2.05...2.2...2.4 V*
Input level, balanced (max):	*1.1 V_{PP}*
Input frequency range (min/max):	*0...300 kHz*
Input resistance, balanced (min):	*200 kΩ*
Input capacitance, balanced (max):	*4 pF*

Modulator Output:	*Value*
Output frequency (min/max):	*85...200 MHz*
Available linear RF power (typ):	*–10 dBm, ZiL=50 kΩ*
Available saturated RF power (typ):	*0 dBm, ZiL=50 kΩ*
Total gain control range (min):	*45 dB*
Gain control slope (typ):	*84 dB/V*
Suppression of 3rd order prods (min):	*35 dB*
Carrier suppression (typ):	*35 dB*
Single sideband suppression:	
Noise floor	*–135 dBm/Hz avg.*
Transmitted I/Q phase balance: drift in whole temperature range:	*–5...5 deg* *–2...2 deg*
Transmitted I/Q amplitude balance: drift in whole temperature range:	*–0.5...0.5 dB* *–0.2...0.2 dB*

Upconversion Mixer

The upconversion mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer upconverts the modulated IF signal coming from quadrature modulator to RF signal.

Parameter:	*Value*
RX frequency range:	*860...915 MHz*
LO frequency range:	*1006...1031 MHz*
IF frequency (nom):	*116 MHz*
Conversion loss (min/typ/max):	*6.0...7.0...8.0 dB*
IIP3 (min):	*0.0 dBm*
LO – RF isolation (min):	*15 dB*
LO power level (max):	*3.0 dBm*

TX Interstage Filters

The TX filters reject the spurious signals generated in the upconversion mixer. They reject the local, image and IF signal leakage and RX band noise, too.

1st TX Buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the upconversion mixer.

Parameter:	*Value*
Operating frequency range:	*890...915 MHz*
Supply voltage (min/typ/max):	*4.25...4.5...2.8 V*
Current consumption (typ/max):	*4.5...5.0 mA*
Insertion gain (min/typ/max):	*11...12...13 dB*
Input VSWR, Zo=50 Ω (max):	*2.0*
Output VSWR, Zo=50 Ω (max):	*2.0*

2nd TX Buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the first interstage filter.

Parameter:	*Value*
Operation frequency range:	*890...915 MHz*
Supply voltage (min/typ/max):	*4.25...4.5...4.8 V*
Current consumption (typ/max):	*9.0...10.0 mA*
Insertion gain (min/typ/max):	*11...12...13 dB*
Output power, Zo=50 Ω (min/typ):	*0...3 dBm*
Input VSWR, Zo=50 Ω (max):	*2.0*
Output VSWR, Zo=50 Ω (max):	*2.0*

Power Amplifier

The power amplifier is a three stage discrete amplifier. It amplifies the 0 dBm TX signal to the desired output level. It has been specified for 6 volts operation.

Parameter:	*Value*
D.C. supply voltage, no RF (max):	*10 V*
D.C. supply voltage (min/typ/max):	*5.3...6.0...8.5 V*
Operation frequency:	*890...915 MHz*
Operating case temp. range (max):	*90 °C*
Max output power (min/typ/max):	*34.5...35...36 dBm, norm cond.*
Max output power (min/typ/max):	*33.5...34...35 dBm, extreme cond.* V_{CC}*=5.4 V, Ta=55°C*

Parameter:	*Value*
Input power (min):	*0 dBm*
Gain (min/typ/max):	*34.5...35...36 dB*
Effiency (typ):	*42 %, Po=35 dBm*
Input VSWR, Zo=50 Ω (max):	*2.0*
Output VSWR, Zo=50 Ω (max):	*2.0*
Harmonics, 2 fo: 3 fo, 4 fo, 5 fo:	*–30 dBc, Po=35 dBm* *–40 dBc, Po=35 dBm*
Noise power (max):	*–114 dBm at receiver band*
Ruggedness (min):	*8 V VSWR=7, P_{OUT}=4 W*
Stability, load VSWR 6:1 (min):	*60 dBc, all spurious*

Power Control Circuitry

The power control loop consists of a power detector and a differential control circuit. The power detector is a combination of a directional coupler and a diode rectifier. The differential control circuit compares the detected voltage and the control voltage (TXC) and controls voltage controlled amplifier (in CRFRT) or the power amplifier. The control circuit is a part of CRFRT.

Parameter:	*Value*
Supply voltage (min/typ/max): using CRFRT:	*4.5...4.7...4.9* *4.27...4.5...4.73*
Supply current (typ/max):	*3.0...5.0 mA*
Power control range (min):	*20 dB*
Power control inaccuracy (max):	*±1.0 dB*
Dynamic range (min):	*80 dB*
Input control voltage range (min/max):	*0.1...2.8 V*

Frequency Synthesizers

The stable frequency source for the synthesizers and base band circuits is discrete voltage controlled crystal oscillator, VCXO in GSM. The frequency of the oscillators is controlled by an AFC voltage, which is generated by the base band circuits. The ON/OFF switching of the oscillator is controlled by the sleep clock in the baseband via VCXOPWR.

The UHF PLL generates the down conversion signal for the receiver and the up conversion signal for the transmitter. The UHF VCO is a discrete oscillator. The working assumption for PLL circuits are from Philips UMA1018 for GSM.

The VHF PLL signal (divided by 4 in CRFR is used as a local for the last mixer. Also the VHF PLL signal (divided by 2 in CRFRT) is used in the I/Q modulator of the transmitter chain.

Frequencies; see RF frequency plan.

Referency Oscillator

In GSM the reference oscillator is a discrete VCXO and the frequency is 13 MHz. The oscillator signal is used for a reference frequency of the synthesizers and the clock frequency for the base band circuits.

Parameter:	*Value*
Centre frequency:	*13 MHz*
Frequency tolerance:	*–18....18 ppm, V_C=2.1 V*
Frequency control range:	*67 ppm*
Supply voltage (min/typ/max):	*4.275...4.5...4.725 V*
Current consumption (typ/max):	*2.5..3.0 mA*
Output voltage (min/typ/max):	*1.3...1.7...2.0 V_{PP}, sine wave for PLLs*
Harmonics (max):	*5 dBc*
Control voltage range (min/max):	*0.3...3.9 V*
Nominal voltage for centre frequency:	*2.1 V*
Control sensitivity (min/typ/max):	*12...18...25 ppm/V*
Frequency stability	
• temperature:	*10 ppm, –25...+75 °C*
• supply voltage:	*1 ppm, 4.7 V ±5 %*
• load:	*0.1 ppm, load ±10 %*
• aging:	*1 ppm, year*
Operating temperature range (min/max):	*–20...70 °C*
Load impedance, resistive part:	*2 kΩ*
parallel capacitance:	*20 pF*

VHF PLL

The VHF PLL consists of the VHF VCO, PLL integrated circuit and loop filter. The output signal is used for the 2nd mixer of the receiver and for the I/Q modulator of the transmitter.

Parameter:	*Value*
Start up setting time (max):	*5 ms*
Phase error (max):	*1 deg., rms*
Sidebands (typ/max)	
• ±200 kHz:	*–75...–70 dB*
• ±400 kHz:	*–84...–70 dB*
• ±1 MHz:	*<–85...–70 dB*
• ±2 MHz:	*<–85...–75 dB*
• ±3 MHz:	*<–85...–85 dB*
• >4 MHz:	*<–85...–85 dB*

VHF VCO + Buffer

The VHF VCO uses a bipolar transistor as a active element and a combination of a chip coil and varactor diode as a resonance circuit. The buffer is combined into the VCO circuit so, that they use same collector current.

Parameter:	*Value*
Supply voltage (min/typ/max):	*4.2...4.5...4.8 V*
Control voltage (min/max):	*0.5...4.0 V*
Supply current (typ/max):	*2.5...5.0 mA*
Operation frequency (typ):	*232 MHz*
Output power level (typ):	*168 mV_{RMS}/1 kΩ*
Control voltage sensitivity (typ):	*12 MHz/V*
Phase noise (max)	
• fo ±200 kHz	*–123 dB*
• fo ±1600 kHz	*–133 dB*
• fo ±3000 kHz	*–143 dB*
Harmonics (typ/max):	*–32...–30 dB*

UHF PLL

The UHF PLL consists of a UHF VCO, divider, PLL circuit and a loop filter. The output signal is used for the 1st mixer of the receiver and the upconversion mixer of the transmitter.

Parameter:	*Value*
Start up setting time (max):	*5 ms*
Phase error (max):	*4 deg., rms*
Settling time ±93 MHz (typ/max):	*525...800 µs*
Sidebands (typ/max)	
• ±200 kHz:	*–80...–60 dB*
• ±400 kHz:	*–87...–65 dB*
• ±600 kHz:	*<–90...–70 dB*
• 1.4...3.0 MHz:	*<–90...–80 dB*
• >3.0 MHz:	*<–80 dB*

UHF VCO + Buffer

The UHF VCO uses a bipolar transistor as a active element and a combination of a microstripline and a varactor diode as a resonance circuit.

UHF VCO Buffers

The UHF VCO output signal is divided into the 1st mixer of the receiver and the upconversion mixer of the transmitter. The UHF VCO signal is amplified after division. There is one buffer for TX and one for RX.

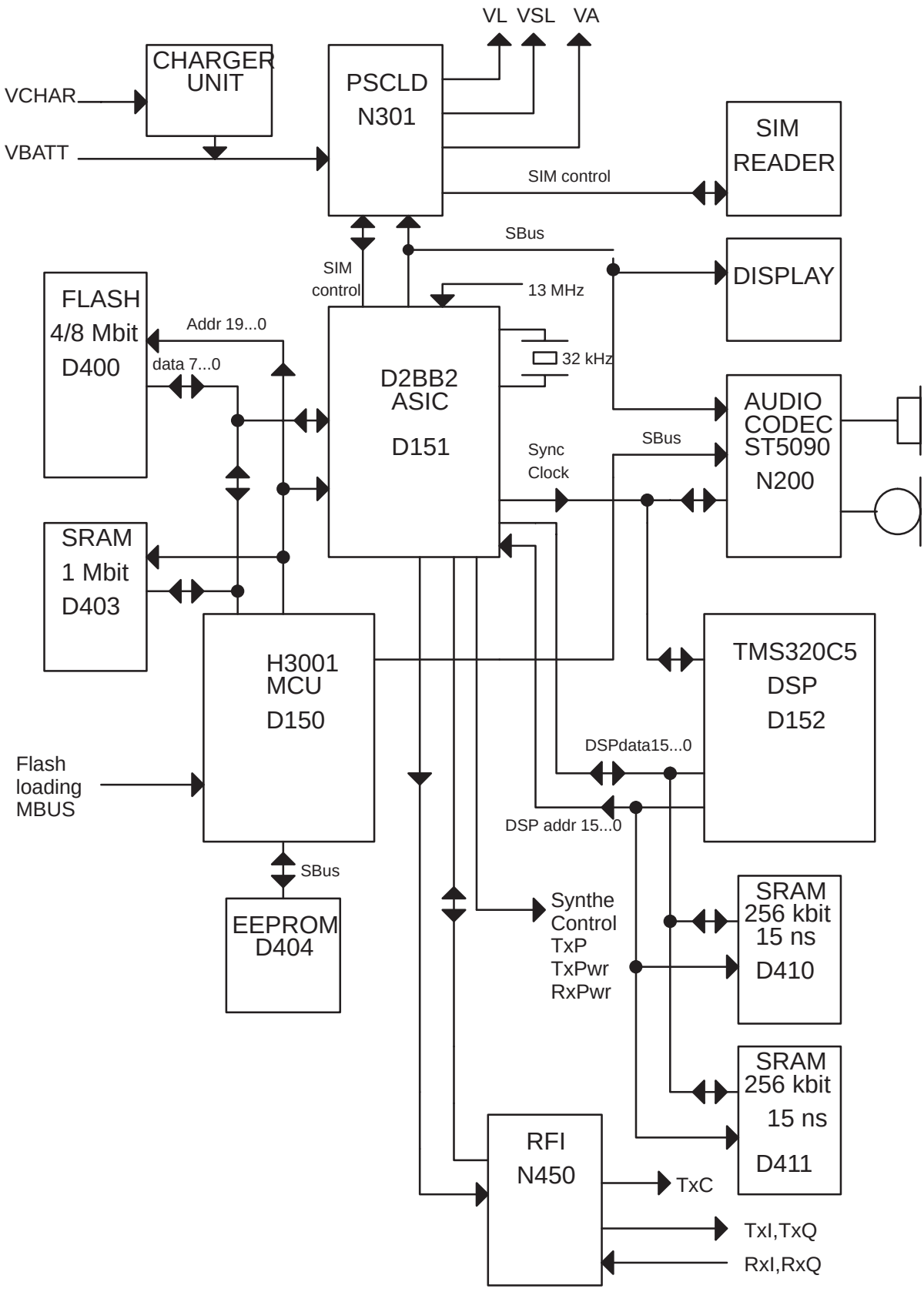
Parameter:	*Value*
Supply voltage (min/typ/max):	*4.2...4.5...4.8 V*
Supply current (typ/max):	*5.5...6.5 mA*
Input power (typ):	*–3 dBm*
Harmonics (max):	*–10 dBc*
Output amplitude (typ):	*700 mV_{RMS}/1 kΩ*

PLL Circuit

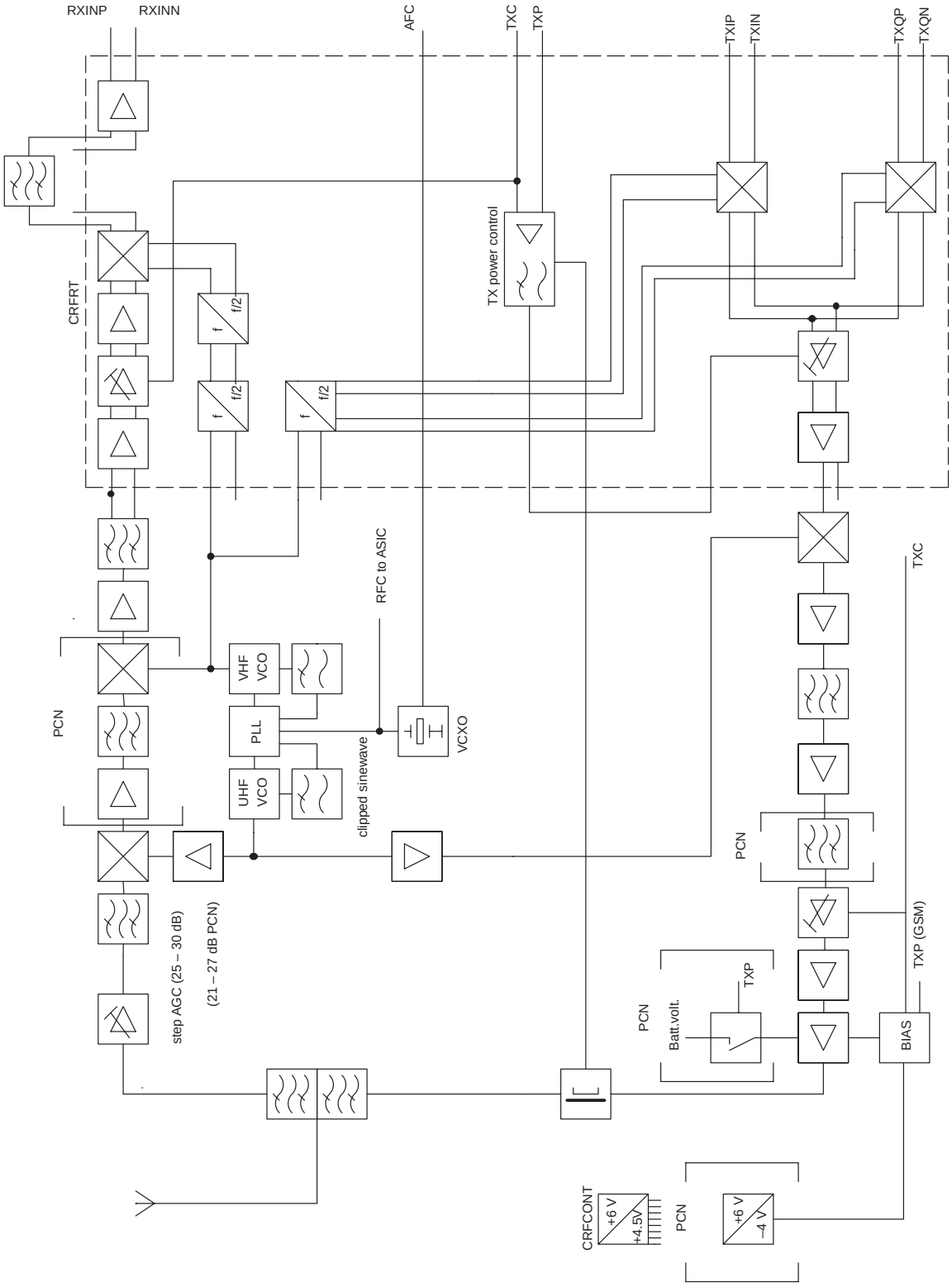
The PLL is PHILIPS UMA1018. The circuit is a dual frequency synthesizer including both the UHF and VHF synthesizers.

Parameter:	*Value*
Supply voltage (min/max):	*2.7...5.5 V*
Supply current (typ):	*8.5 mA*
Principal input frequency (min/max):	*500...1200 MHz, V_{DD} = 4.5 V*
Auxiliary input frequency (min/max):	*20...300 MHz, V_{DD} = 4.5 V*
Input reference frequency (min/max):	*3...40 MHz, V_{DD} = 4.5 V*
Input signal level (min/max):	*50...500 mV_{RMS}*

Interconnection Diagram of Baseband

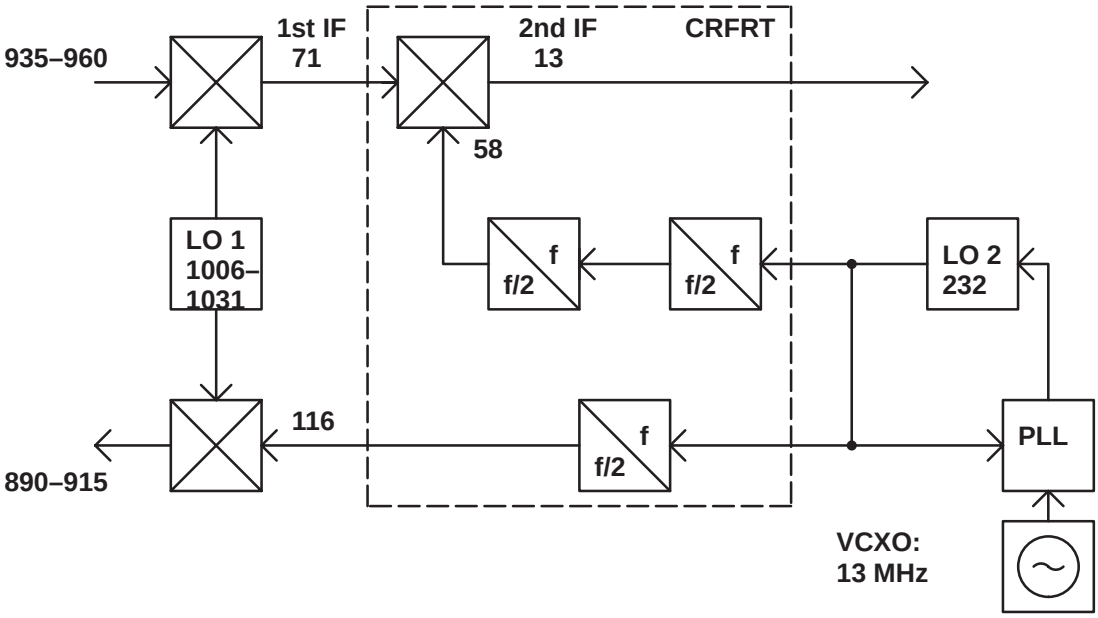


Block Diagram of RF



RF Frequency Plan

GSM



Power Distribution Diagram of RF

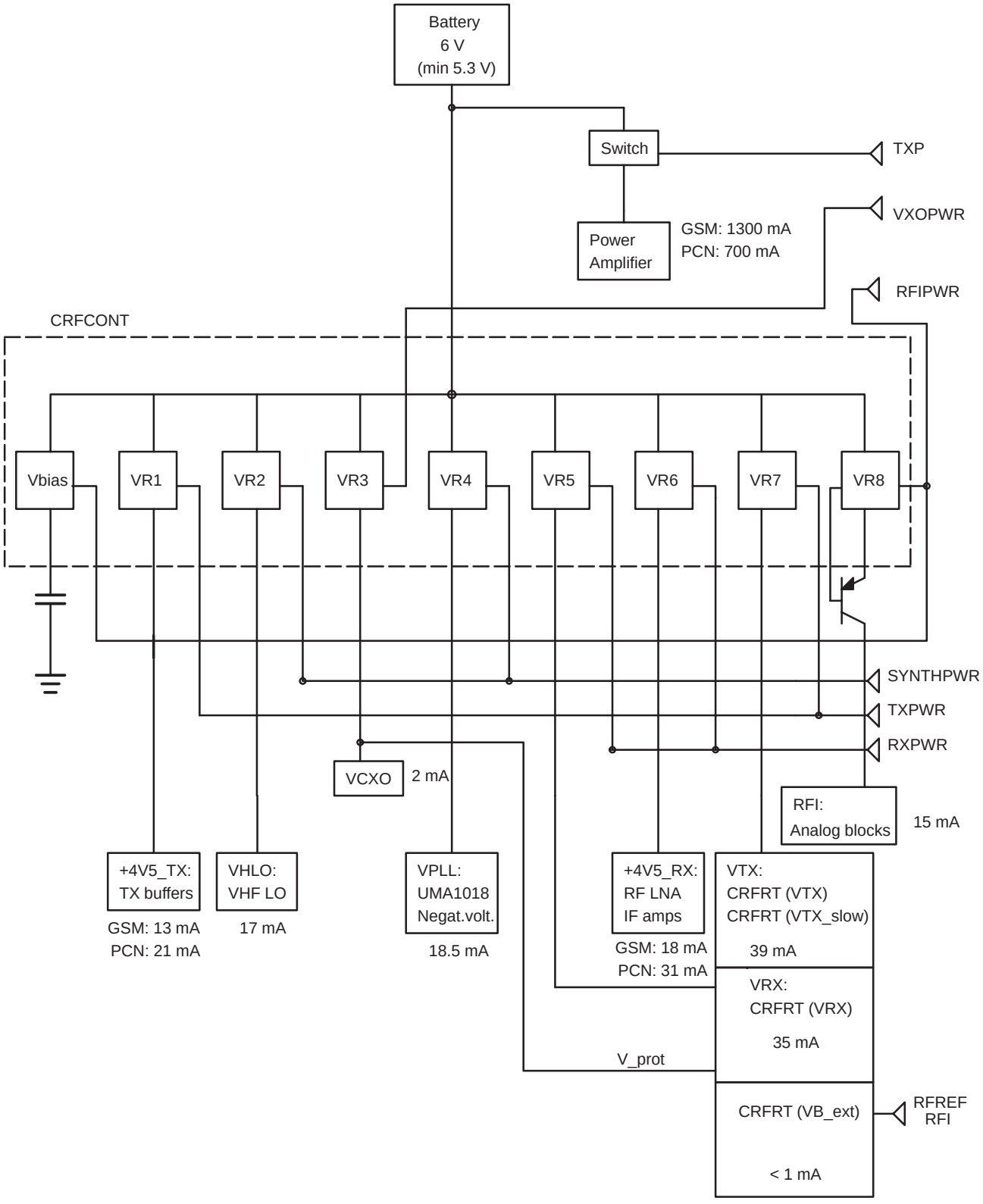
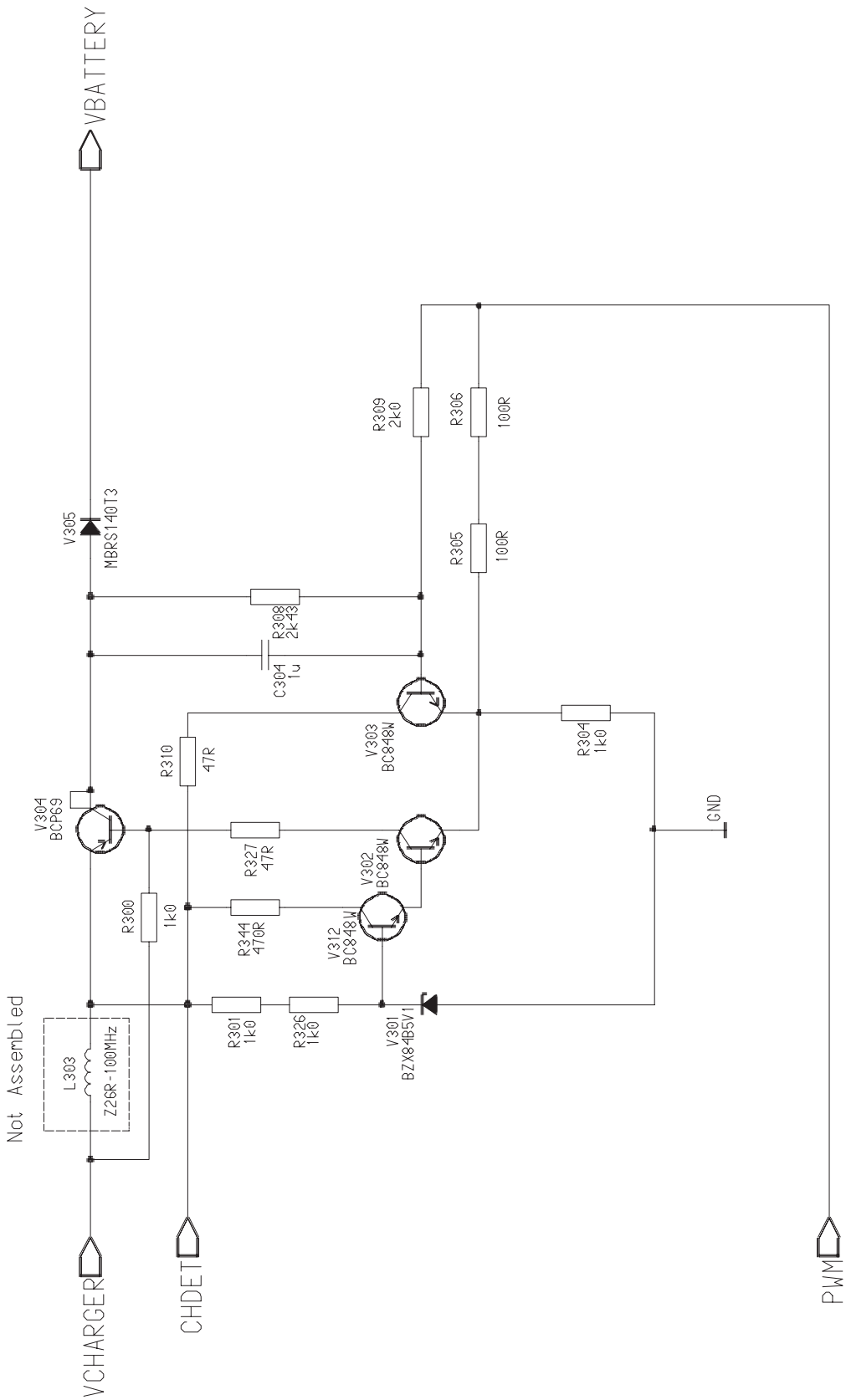
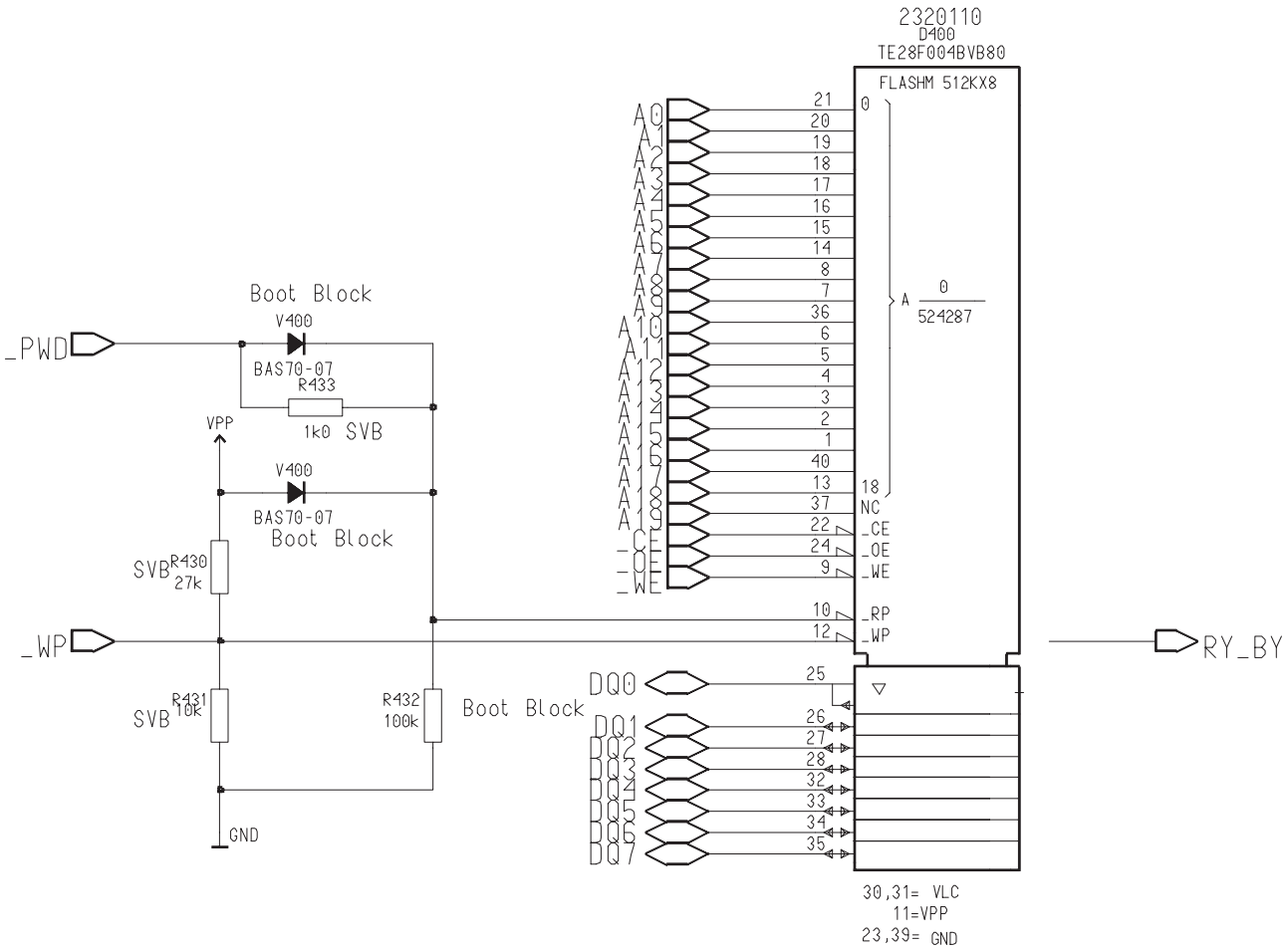


Figure 1. Power distribution diagram

Circuit Diagram of Charger Control (Version 1.0 ; Edit 15)



Circuit Diagram of 4 MBit Flash Memory (Version 3.0 ; Edit 22)



Block Diagram of Baseband

Circuit Diagram of Power Supply & Charging

Circuit Diagram of Central Processing Unit

Circuit Diagram of MCU Memory Block

Circuit Diagram of Keyboard & Display Interface

Circuit Diagram of Audio

Circuit Diagram of DSP Memory Block

Circuit Diagram of RFI

Circuit Diagram of Receiver

Circuit Diagram of Transceiver

Layout Diagrams of GT8

Layout Diagrams of GT8

Parts list of GT8 (EDMS Issue 4.5)

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R150	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R151	1430718	Chip resistor	47	5 % 0.063 W 0402
R152	1430718	Chip resistor	47	5 % 0.063 W 0402
R155	1430726	Chip resistor	100	5 % 0.063 W 0402
R156	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R161	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R166	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R168	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R201	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R202	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R203	1430726	Chip resistor	100	5 % 0.063 W 0402
R204	1430726	Chip resistor	100	5 % 0.063 W 0402
R205	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R206	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R207	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R208	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R209	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R210	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R211	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R212	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R214	1430710	Chip resistor	22	5 % 0.063 W 0402
R215	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R216	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R217	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R218	1430710	Chip resistor	22	5 % 0.063 W 0402
R219	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R220	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R222	1430700	Chip resistor	10	5 % 0.063 W 0402
R223	1430700	Chip resistor	10	5 % 0.063 W 0402
R250	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R251	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R252	1430716	Chip resistor	39	5 % 0.063 W 0402
R253	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R254	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R255	1430724	Chip resistor	82	5 % 0.063 W 0402
R256	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R257	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R258	1430726	Chip resistor	100	5 % 0.063 W 0402
R259	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R260	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R261	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R262	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R263	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

R264	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R265	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R266	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R267	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R268	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R269	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R270	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R271	1430061	Chip resistor	511 k	1 % 0.063 W 0603
R272	1430113	Chip resistor	348 k	1 % 0.063 W 0603
R300	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R301	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R302	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R303	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R304	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R305	1430726	Chip resistor	100	5 % 0.063 W 0402
R306	1430726	Chip resistor	100	5 % 0.063 W 0402
R307	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R308	1430027	Chip resistor	2.43 k	1 % 0.063 W 0603
R309	1430025	Chip resistor	2.0 k	1 % 0.063 W 0603
R310	1430718	Chip resistor	47	5 % 0.063 W 0402
R311	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R312	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R313	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R314	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R315	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R316	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R317	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R318	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R319	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R320	1430726	Chip resistor	100	5 % 0.063 W 0402
R321	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R322	1430726	Chip resistor	100	5 % 0.063 W 0402
R323	1430726	Chip resistor	100	5 % 0.063 W 0402
R324	1430718	Chip resistor	47	5 % 0.063 W 0402
R326	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R327	1430718	Chip resistor	47	5 % 0.063 W 0402
R328	1430726	Chip resistor	100	5 % 0.063 W 0402
R329	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R330	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R331	1430718	Chip resistor	47	5 % 0.063 W 0402
R332	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R334	1430718	Chip resistor	47	5 % 0.063 W 0402
R336	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R337	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R340	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R343	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R344	1430744	Chip resistor	470	5 % 0.063 W 0402
R345	1430804	Chip resistor	100 k	5 % 0.063 W 0402

R348	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R349	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R400	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R401	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R402	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R403	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R404	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R405	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R406	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R407	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R408	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R409	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R410	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R411	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R412	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R413	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R415	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R416	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R430	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R431	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R433	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R452	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R453	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R454	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R455	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R501	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R502	1430732	Chip resistor	180	5 % 0.063 W 0402
R503	1430732	Chip resistor	180	5 % 0.063 W 0402
R504	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R505	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R507	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R508	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R509	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R511	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R512	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R513	1430740	Chip resistor	330	5 % 0.063 W 0402
R514	1430710	Chip resistor	22	5 % 0.063 W 0402
R541	1430710	Chip resistor	22	5 % 0.063 W 0402
R542	1430734	Chip resistor	220	5 % 0.063 W 0402
R543	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R544	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R545	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R546	1430724	Chip resistor	82	5 % 0.063 W 0402
R547	1430744	Chip resistor	470	5 % 0.063 W 0402
R551	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R552	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R553	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R554	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402

R555	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R556	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R557	1430732	Chip resistor	180	5 % 0.063 W 0402
R558	1430730	Chip resistor	150	5 % 0.063 W 0402
R559	1430740	Chip resistor	330	5 % 0.063 W 0402
R560	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R562	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R566	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R570	1430726	Chip resistor	100	5 % 0.063 W 0402
R571	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R572	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R573	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R574	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R578	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R579	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R580	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R583	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R601	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R602	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R603	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R701	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R702	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R703	1430710	Chip resistor	22	5 % 0.063 W 0402
R704	1430740	Chip resistor	330	5 % 0.063 W 0402
R705	1430724	Chip resistor	82	5 % 0.063 W 0402
R708	1430690	Chip jumper		0402
R711	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R712	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R713	1430744	Chip resistor	470	5 % 0.063 W 0402
R714	1430700	Chip resistor	10	5 % 0.063 W 0402
R715	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R716	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R717	1430734	Chip resistor	220	5 % 0.063 W 0402
R725	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R726	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R727	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R728	1430730	Chip resistor	150	5 % 0.063 W 0402
R736	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R737	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R738	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R739	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R740	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R741	1430746	Chip resistor	560	5 % 0.063 W 0402
R742	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R743	1430700	Chip resistor	10	5 % 0.063 W 0402
R744	1430734	Chip resistor	220	5 % 0.063 W 0402
R755	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R756	1412279	Chip resistor	2.2	5 % 0.1 W 0805

R765	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R766	1430748	Chip resistor	680	5 % 0.063 W 0402
R767	1430732	Chip resistor	180	5 % 0.063 W 0402
R768	1430752	Chip resistor	820	5 % 0.063 W 0402
R769	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R780	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R781	1430740	Chip resistor	330	5 % 0.063 W 0402
R782	1430726	Chip resistor	100	5 % 0.063 W 0402
R784	1430726	Chip resistor	100	5 % 0.063 W 0402
R785	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R800	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R801	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R802	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R803	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R804	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R805	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R806	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R807	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R808	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R811	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R820	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R821	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R822	1430798	Chip resistor	56 k	5 % 0.063 W 0402
R823	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R824	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R825	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R826	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R827	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R828	1430786	Chip resistor	18 k	5 % 0.063 W 0402
R829	1430718	Chip resistor	47	5 % 0.063 W 0402
R830	1430726	Chip resistor	100	5 % 0.063 W 0402
R840	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R841	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R842	1430844	Chip resistor	3.9 k	1 % 0.063 W 0402
R843	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R844	1430734	Chip resistor	220	5 % 0.063 W 0402
R845	1430700	Chip resistor	10	5 % 0.063 W 0402
R846	1430726	Chip resistor	100	5 % 0.063 W 0402
R847	1430718	Chip resistor	47	5 % 0.063 W 0402
R860	1430716	Chip resistor	39	5 % 0.063 W 0402
C151	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C153	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C154	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C155	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C156	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C158	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C159	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C160	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206

C161	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C162	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C165	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C166	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C167	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C168	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C169	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C170	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C200	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C201	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C202	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C203	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C204	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C205	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C206	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C207	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C208	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C211	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C212	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C213	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C214	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C215	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C216	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C217	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C218	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C220	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C221	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C222	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C223	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C224	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C225	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C250	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C261	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C262	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C263	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C264	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C265	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C266	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C267	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C268	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C300	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C301	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C302	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C303	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C304	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C305	2604431	Tantalum cap.	10 µ	20 % 16 V 6.0x3.2x2.8
C306	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C307	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206

C308	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C309	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C310	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C311	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C312	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C313	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C314	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C315	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C316	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C317	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C318	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C319	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C320	2610153	Tantalum cap.	10 µ	20 % 6.0x3.2x2.5
C321	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C322	2610153	Tantalum cap.	10 µ	20 % 6.0x3.2x2.5
C323	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C324	2610153	Tantalum cap.	10 µ	20 % 6.0x3.2x2.5
C325	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C326	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C328	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C329	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C330	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C331	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C334	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C335	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C337	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C338	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C339	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C341	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C400	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C401	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C402	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C403	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C404	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C410	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C411	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C412	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C413	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C414	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C450	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C451	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C452	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C453	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C456	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C457	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C458	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C459	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C460	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206

C462	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C501	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C502	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C503	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C504	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C505	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C506	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C511	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C512	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C513	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C514	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C515	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C516	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C517	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C521	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C536	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C541	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C542	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C543	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C544	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C545	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C546	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C551	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C552	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C553	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C554	2320566	Ceramic cap.	180 p	5 % 50 V 0402
C555	2320566	Ceramic cap.	180 p	5 % 50 V 0402
C556	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C557	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C558	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C559	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C560	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C561	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C562	2320075	Ceramic cap.	470 p	5 % 50 V 0603
C563	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C566	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C569	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C570	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C571	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C572	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C573	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C574	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C575	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C580	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C601	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C602	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C603	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C604	2310784	Ceramic cap.	100 n	10 % 25 V 0805

C605	2312410	Ceramic cap.	1.0 µ	10 % 16 V 1206
C607	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C608	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C609	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C610	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C701	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C702	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C703	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C704	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C705	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C710	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C711	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C712	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C713	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C716	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C720	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C721	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C722	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C723	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C725	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C726	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C728	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C730	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C731	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C732	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C735	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C736	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C737	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C738	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C739	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C740	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C741	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C742	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C743	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C744	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C755	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C756	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C757	2320578	Ceramic cap.	560 p	5 % 50 V 0402
C758	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C759	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C760	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C761	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C762	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C764	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C768	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C770	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C780	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C781	2320536	Ceramic cap.	10 p	5 % 50 V 0402

C782	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C783	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C784	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C800	2604079	Tantalum cap.	0.22 µ	20 % 35 V 3.2x1.6x1.6
C801	2310752	Ceramic cap.	10 n	20 % 50 V 0805
C802	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C803	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C804	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C805	2320728	Ceramic cap.	220 p	10 % 50 V 0402
C806	2610100	Tantalum cap.	1 µ	20 % 10 V 2.0x1.3x1.2
C807	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C809	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C820	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C821	2313104	Ceramic cap.	1.0 n	2 % 50 V 1206
C822	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C823	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C824	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C828	2610100	Tantalum cap.	1 µ	20 % 10 V 2.0x1.3x1.2
C829	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C830	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C831	2610100	Tantalum cap.	1 µ	20 % 10 V 2.0x1.3x1.2
C832	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C840	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C841	2610100	Tantalum cap.	1 µ	20 % 10 V 2.0x1.3x1.2
C842	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C843	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C844	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C845	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C846	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C847	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C848	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C849	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C850	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C851	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C862	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C863	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
L151	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L152	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L153	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L200	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L201	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L202	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L203	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L204	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L205	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L206	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L207	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L208	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A

L300	3606946	Ferrite bead		0.2Ω 26Ω/100MHz 1206
L301	3606946	Ferrite bead		0.2Ω 26Ω/100MHz 1206
L302	3606946	Ferrite bead		0.2Ω 26Ω/100MHz 1206
L304	3606946	Ferrite bead		0.2Ω 26Ω/100MHz 1206
L307	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L308	3606946	Ferrite bead		0.2Ω 26Ω/100MHz 1206
L310	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L311	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L410	3640011	Filter	Z>600Ω/100M	0.6Ω max 0.2 A
L511	3641550	Chip coil	120 n	10 % Q=35 0805
L532	3641550	Chip coil	120 n	10 % Q=35 0805
L541	3641550	Chip coil	120 n	10 % Q=35 0805
L542	3608326	Chip coil	330 n	5 % 1206
L543	3641560	Chip coil	220 n	10 % Q=30/100 MHz 0805
L544	3641560	Chip coil	220 n	10 % Q=30/100 MHz 0805
L545	3608326	Chip coil	330 n	5 % 1206
L546	3608326	Chip coil	330 n	5 % 1206
L551	3641538	Chip coil	39 n	20 % Q=40 0805
L700	3606946	Ferrite bead		0.2Ω 26Ω/100MHz 1206
L705	3640013	Chip coil	8 n	5 % Q=50/250 MHz 0805
L710	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L711	3641542	Chip coil	56 n	10 % Q=40 0805
L800	3641324	Chip coil	10 µ	10 % Q=25/2.52 MHz 1008
L840	3641574	Chip coil	68 n	5 % Q=40 0805
L841	3641538	Chip coil	39 n	20 % Q=40 0805
L842	3641558	Chip coil	8 n	10 % Q=50 0805
B150	4510029	Crystal	32.768 k	20PPM 20PPM
B800	4510075	Crystal	13.000 M	+–5/TSTAB+–7PPM
G001	4352933	Vco	1006–1031 MHz	4.5 V 15 mA
Z500	4512046	SM, dupl.	890–915/935–960 MHz	
Z505	4511016	Saw filter	947.5±12.5 M	RXJP
Z541	4511026	SM, SAW IF filter		71 MHz 10 dBm
Z551	4510009	SM, cer.bpf	13 MHz±90kHz/1 dB	330Ω
Z713	4550101	SM, cer bpf	902.5±12.5MHz	tx
V200	4210100	Transistor	BC848W	npn 30 V SOT323
V201	4210100	Transistor	BC848W	npn 30 V SOT323
V202	4210100	Transistor	BC848W	npn 30 V SOT323
V203	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V250	4864370	Led	Green	1208
V251	4864370	Led	Green	1208
V252	4864378	Led	Green	V 0805
V253	4864378	Led	Green	V 0805
V254	4864378	Led	Green	V 0805
V255	4864378	Led	Green	V 0805
V256	4864370	Led	Green	1208
V257	4864370	Led	Green	1208
V258	4864378	Led	Green	V 0805
V259	4864378	Led	Green	V 0805

V260	4864378	Led	Green	V 0805
V261	4864378	Led	Green	V 0805
V262	4210100	Transistor	BC848W	npn 30 V SOT323
V263	4210100	Transistor	BC848W	npn 30 V SOT323
V264	4210100	Transistor	BC848W	npn 30 V SOT323
V300	4110028	Trans. supr.	16V	23 A 600 W DO214AA
V301	4110130	Zener diode	BZX84	2 % 5.1 V 0.3 W SOT23
V302	4210100	Transistor	BC848W	npn 30 V SOT323
V303	4210100	Transistor	BC848W	npn 30 V SOT323
V304	4210092	Transistor		SOT223
V305	4110034	Schottky diode	MBRS140	40 V 1 A DO214AA
V306	4210092	Transistor		SOT223
V307	4219928	TR+RX2	RN2302	p 50V 50mA 10k
V308	4219926	TR+RX2	RN2302	p 50V 50mA 10k
V309	4219926	TR+RX2	RN2302	p 50V 50mA 10k
V310	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MW
V312	4210100	Transistor	BC848W	npn 30 V SOT323
V450	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MW
V501	4210046	Transistor	BFP182	npn 20 V 35 mA SOT143
V502	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MW
V503	4210100	Transistor	BC848W	npn 30 V SOT323
V511	4115802	Sch. diode x 2	4V	30 mA SOT23
V512	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V541	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V701	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V702	4100567	Sch. diode x 2	BAS70–04	70V15 mA SERSOT23
V710	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23
V725	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23
V726	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MW
V735	4210100	Transistor	BC848W	npn 30 V SOT323
V736	4217070	Transistor x 2		IMD
V737	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MW
V738	4210090	Transistor	BFG540/X	npn 15 V 129 mA SOT143
V755	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MW
V756	4210133	Transistor	BFG10W/X	npn 10 V 0.25 A SOT343
V765	4210100	Transistor	BC848W	npn 30 V SOT323
V766	4210100	Transistor	BC848W	npn 30 V SOT323
V767	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V768	4210135	Transistor	BLT82	npn 10 V SO8S
V780	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V800	4111092	Cap. diode	BB639	30 V SOD323
V801	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V802	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V840	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V841	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V842	4110018	Cap. diode	BB135	30 V SOD323
D150	4340307	IC, MCU		TQFP80
D151	4370124	Cf70131 gsm/pcn asic bart		SQFP144

D152	4371025	IC, tms320lc541/d36818 gh4 DSP	SQF100
D400	4340305	IC, 512kx8 110ns 3V E28F004BVBT	SO40
D402	4340045	IC, SRAM	TSO28
D404	4343280	IC, EEPROM	2kx8 bit SO8S
D410	4340045	IC, SRAM	TSO28
D411	4340045	IC, SRAM	TSO28
N200	4340013	St5090 audio codec	SO28W
N301	4370199	Stt225b pscld–c pw supply	QFP44
N450	4370207	St7522 rfi2 v2.2 tdma codec	QFP64
N551	4370091	Crfrt_st tx.mod+rxif+pwc	SQFP44
N601	4370095	Crfcontf 8xreg4.5v vref2v5	VSOP28
N820	4340069	IC, 2xsynth 3v UMA1018M/C1/S1	SSO20
X100	5409019	SM, fpc connector	24 poles p 0.8
X101	5460007	20 pole spring type direct board	
X102	5408807	Sim card reader ccm04–5002	3CO2x3con
X103	5469001	System connector	
X501	9510245	Antenna clip	3D25495 NHE–5NX
	9854060	PC board GT8	48.3x150.4x1.0 m6 3/pa

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